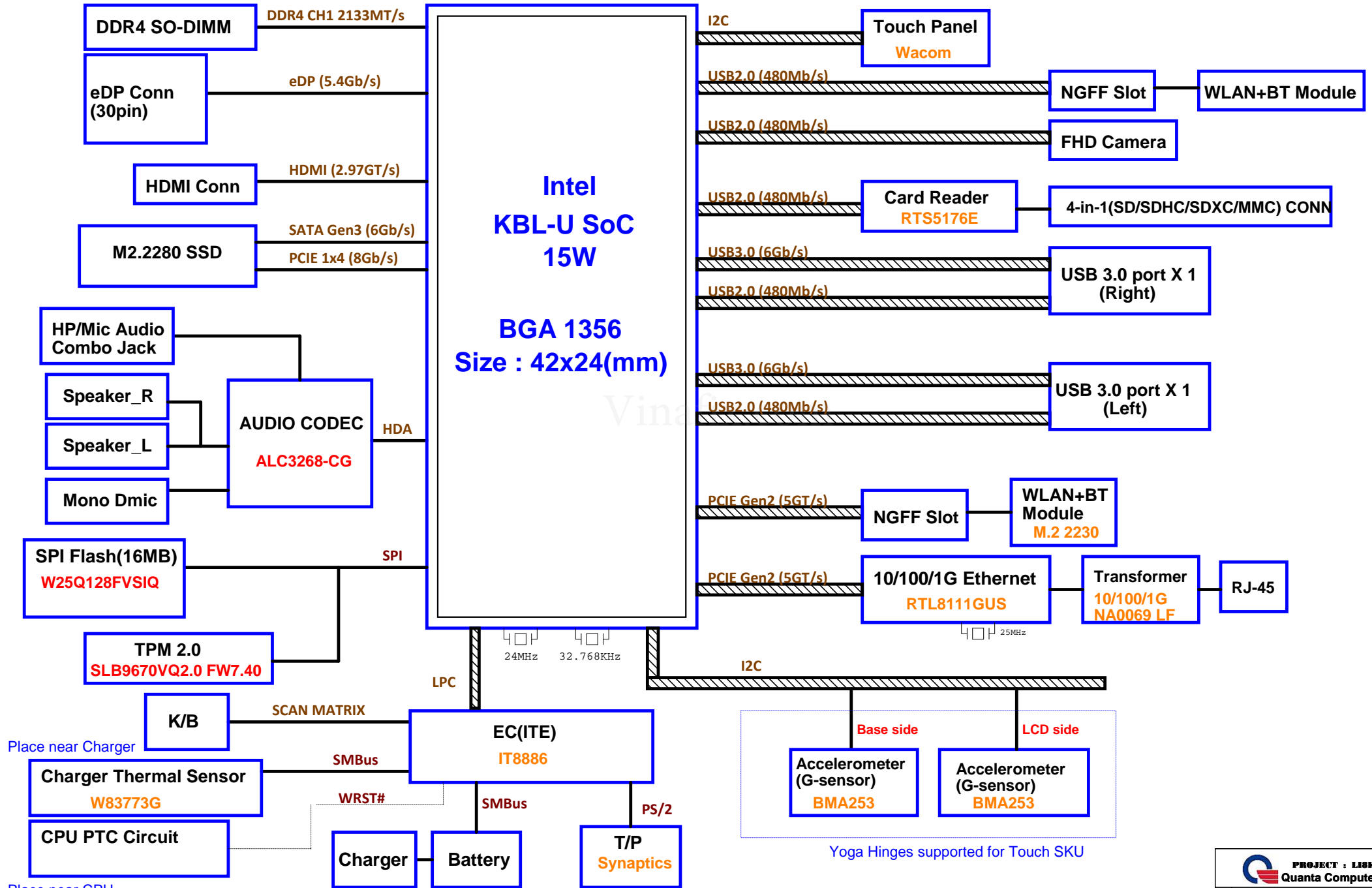
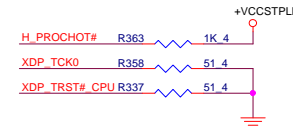
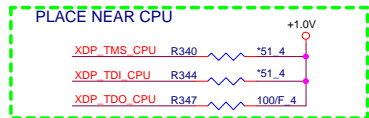
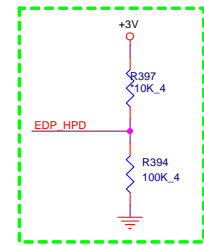


Newton II Intel Kaby lake-U Platform UMA Block Diagram (Windows)



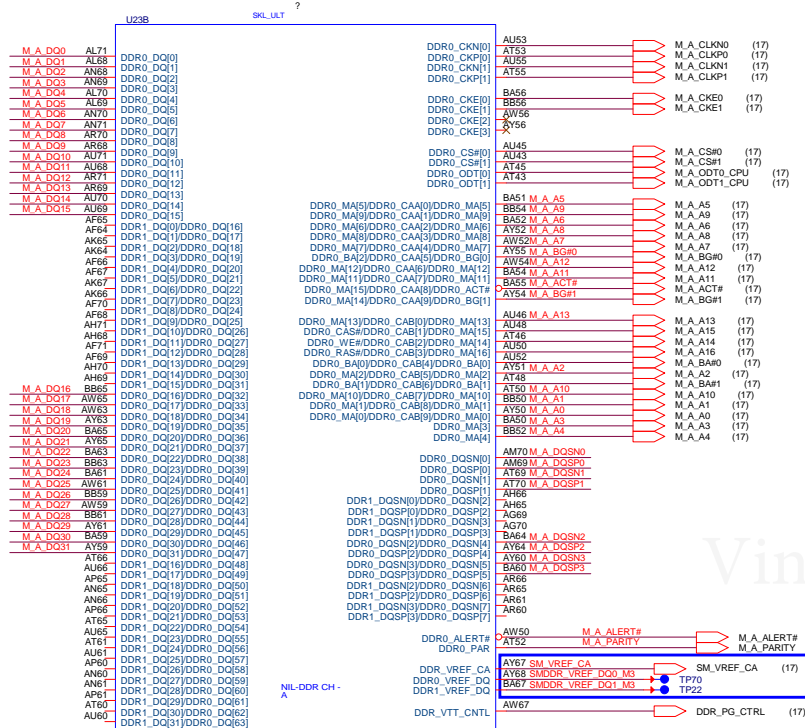


(17) M_A_DQSN[7:0]
(17) M_A_DQSP[7:0]
(17) M_A_DQ[63:0]

Kabylake ULT Processor (DDR4)

—  +1.2V_SUS (6,17,38,44)

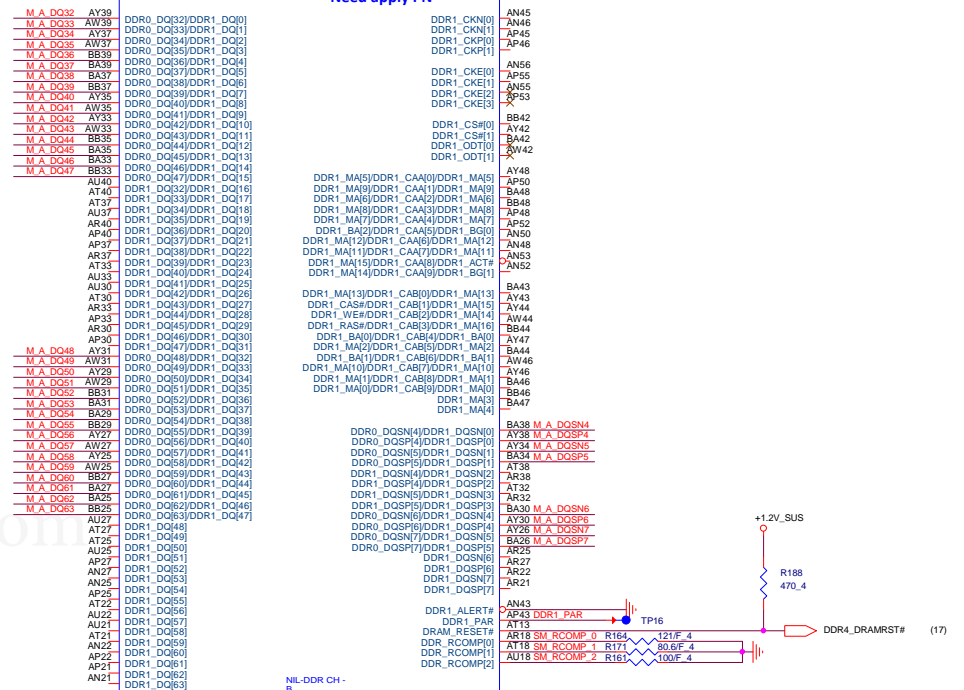
Need apply PN

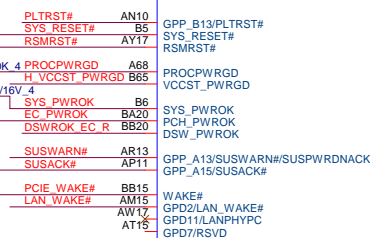
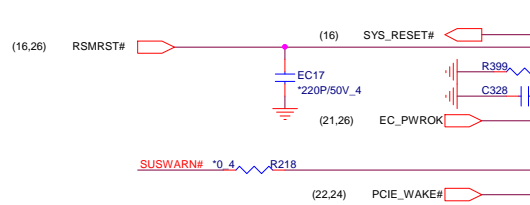
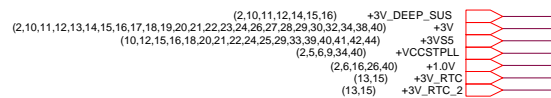


Vinafix.com

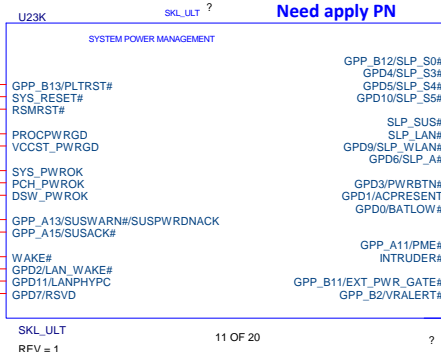
SKL_ULT

Need apply PN

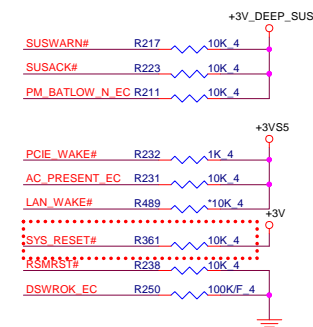




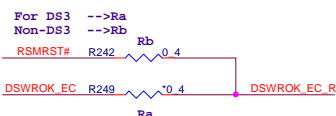
Need apply PN



PCH Pull-high/low(CLG)

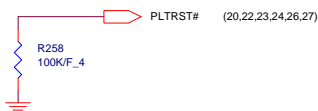


For DS3 Sequence

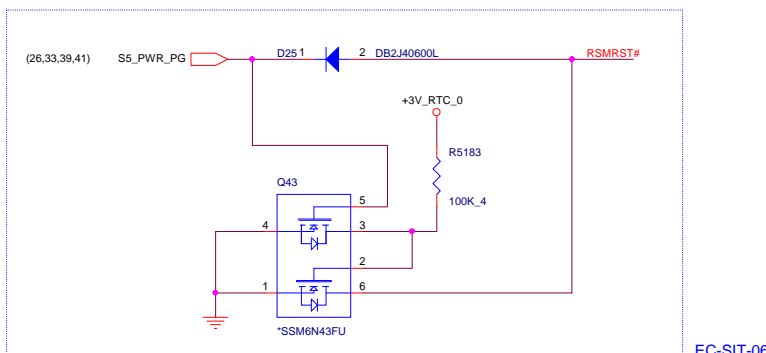
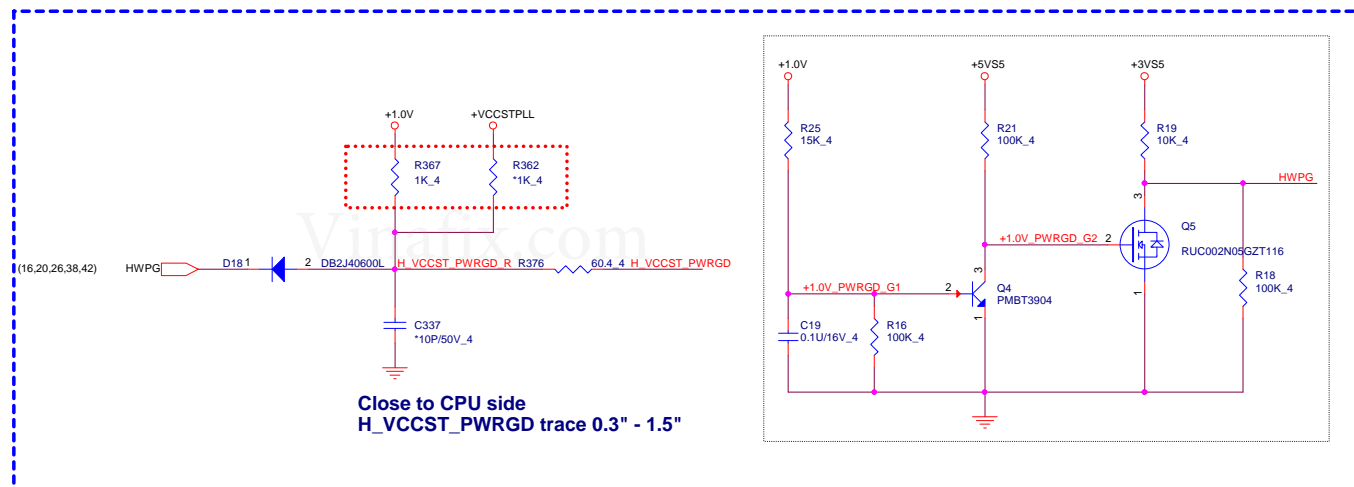


PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns



System PWR_OK(CLG)



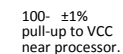
EC-SIT-06



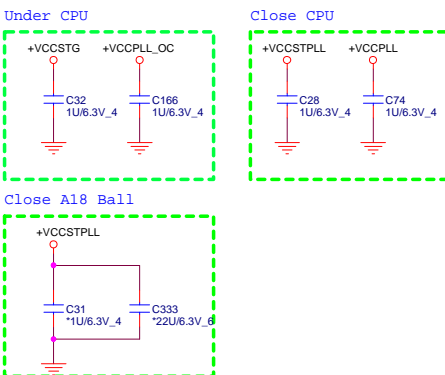
PROJECT : L18K
Quanta Computer Inc.

Size Document Number Custom 04 -- SKYPAKE 5/20(Power Manger) Rev 3A

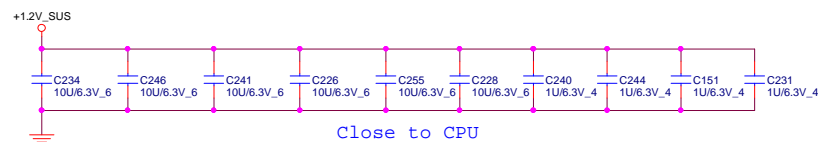
Date: Thursday, September 08, 2016 Sheet 4 of 45

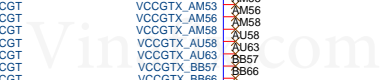



**CLOSE TO CPU
PLACE THE PU RESISTORS**

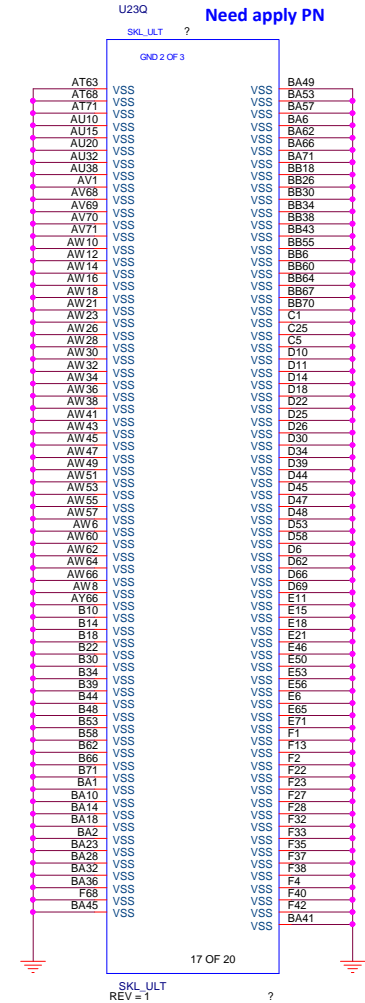
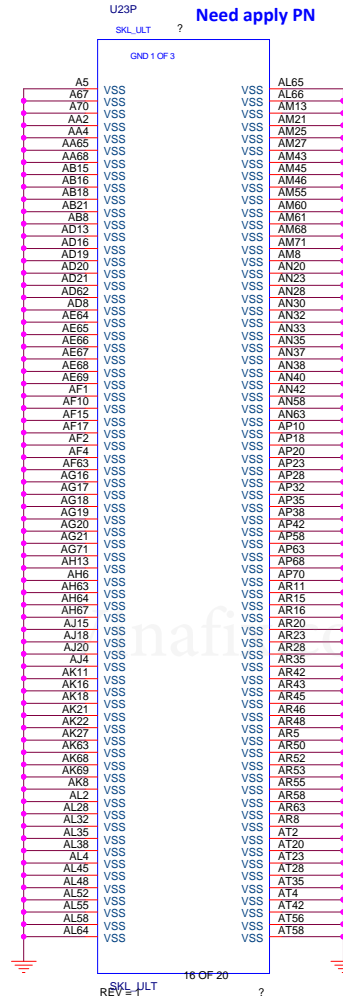
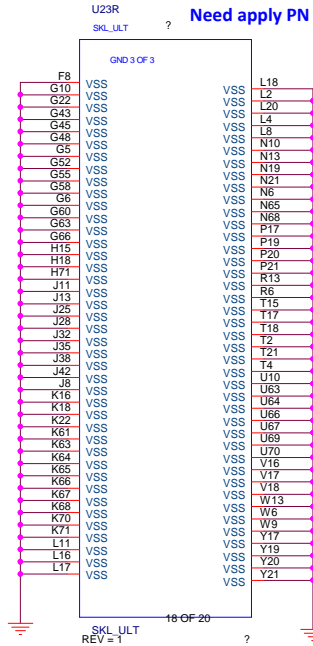


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

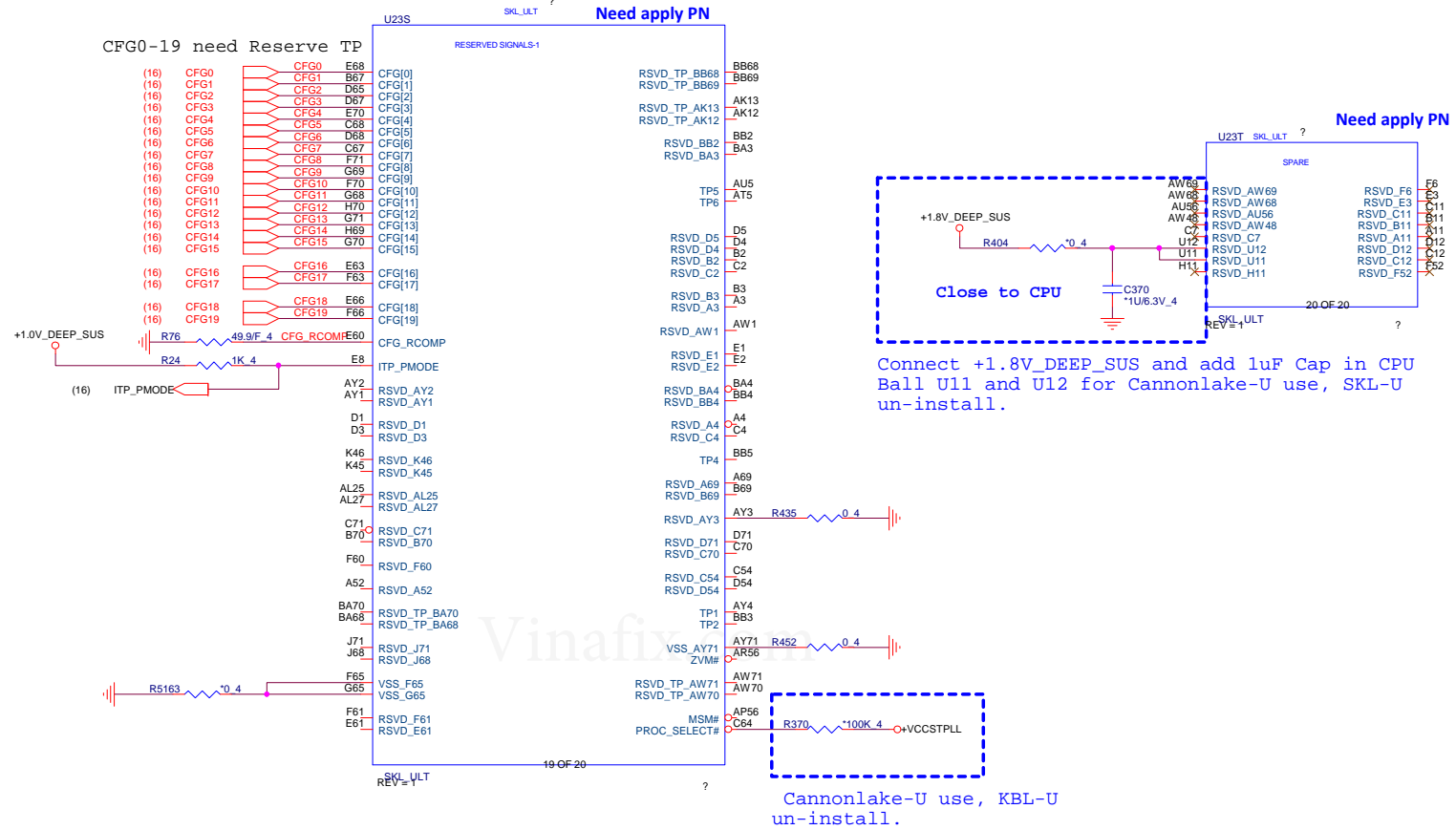




 <div style="display: inline-block; vertical-align: middle;"> PROJECT : LI3K Quanta Computer Inc. </div>			
Size	Document Number	07 -- SKYPAKE 8/20 (POWER-3)	Rev 3A
Date:	Thursday, September 08, 2016	Sheet 7 of 45	



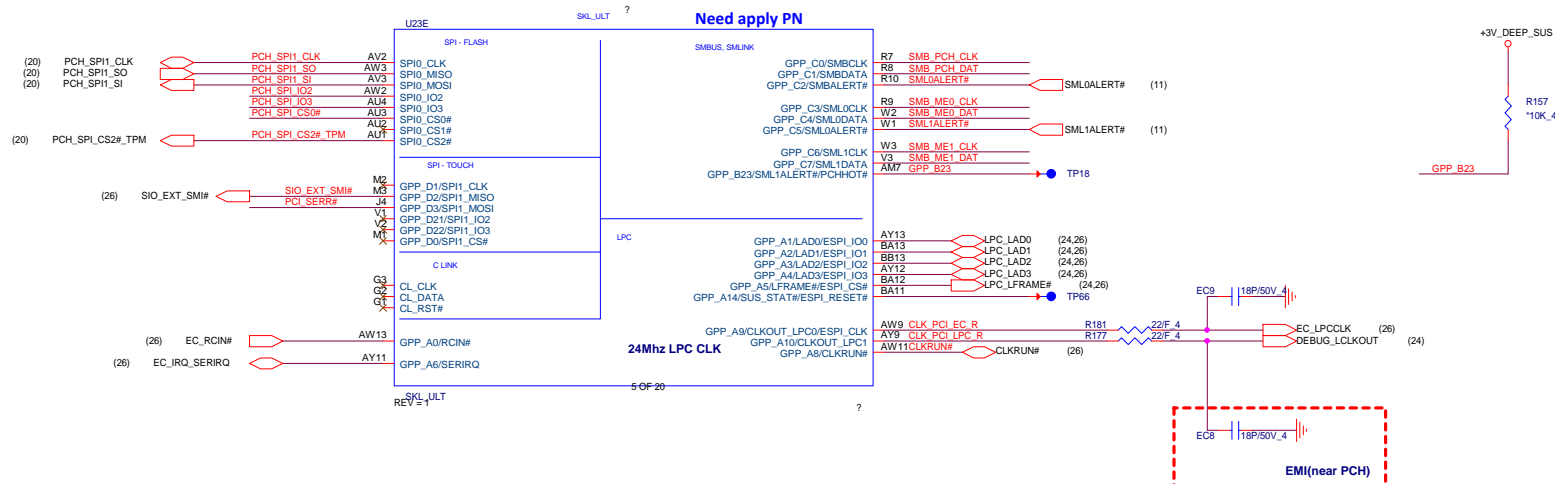
+1.0V_DEEP_SUS (13,15,16,39,40,44)
+VCCSTPLL (2,4,5,6,34,40)



Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R398 ~1K 4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R401 ~1K 4

+3V_DEEP_SUS (2,4,11,12,14,15,16)
+3V (2,4,11,12,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,32,34,38,40)
+3VSS (4,12,15,16,18,20,21,22,24,25,29,33,39,40,41,42,44)



Vinafix.com

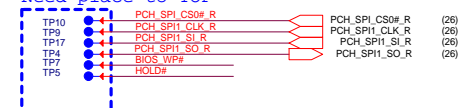
GPIO Pull UP



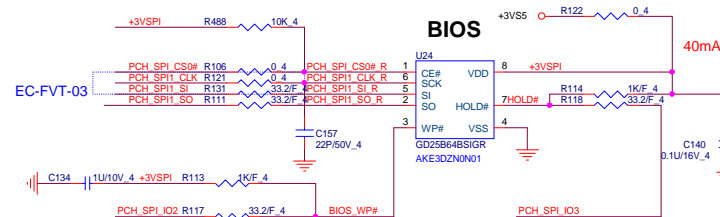
PCH SPI ROM(CLG)

Vender	Size	P/N
EON	16MB	AKE3DZNKQ00(EN25QH128AHIP)
Winbond	16MB	AKE3DZN0N01(W25Q128FVSIQ)
Socket		DFHS08FS023

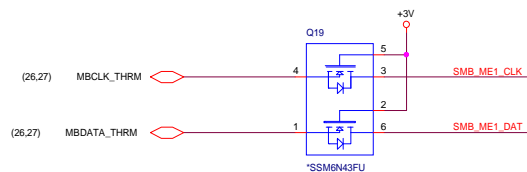
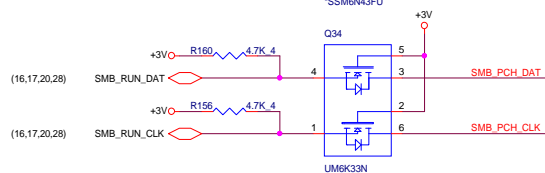
Need place to TOP



PCH SPI ROM(CLG)



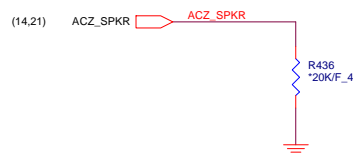
SMBus/Pull-up(CLG)

Thermal sensor
ECTouch Pad
XDP
DDR4

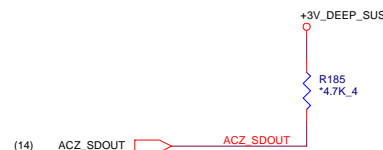
+3V_DEEP_SUS (2,4,10,12,14,15,16)
+3V (2,4,10,12,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,32,34,38,40)

Functional Strap Definitions

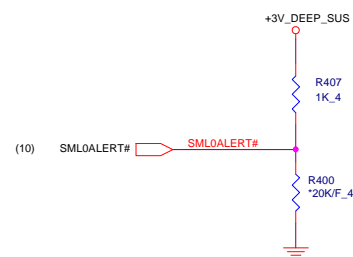
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



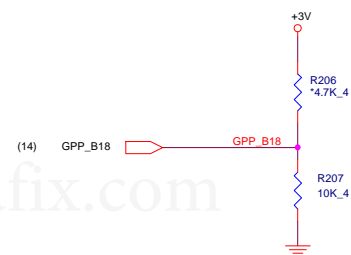
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



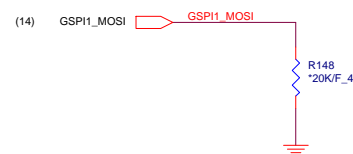
Flash Descriptor Security Override:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



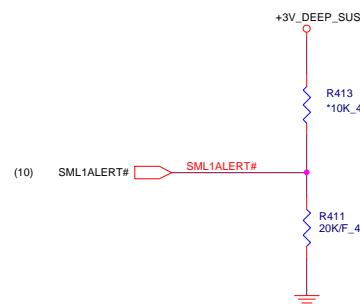
TLS Confidentiality:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



Boot BIOS Strap Bit :
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC



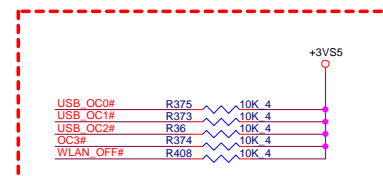
eSPI or LPC:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.



PROJECT : L18K
Quanta Computer Inc.

Size Document Number 11 -- SKYPAKE 15/20(HDA) Rev 3A

Date: Thursday, September 08, 2016 Sheet 11 of 45



USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 Conn-L
PORT-2	Cobime USB3.0 Conn-R
PORT-3	Camera
PORT-4	Cardreader
PORT-5	NC
PORT-6	NC
PORT-7	Bluetooth
PORT-8	NC
PORT-9	NC
PORT-10	NC



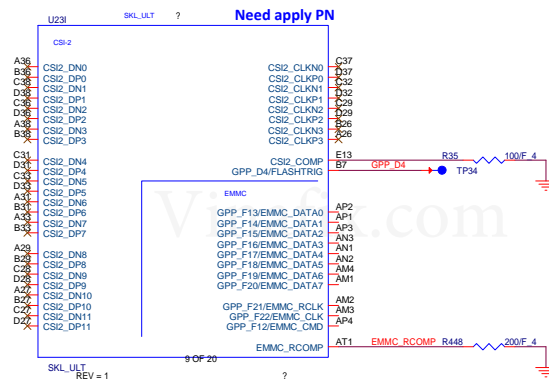
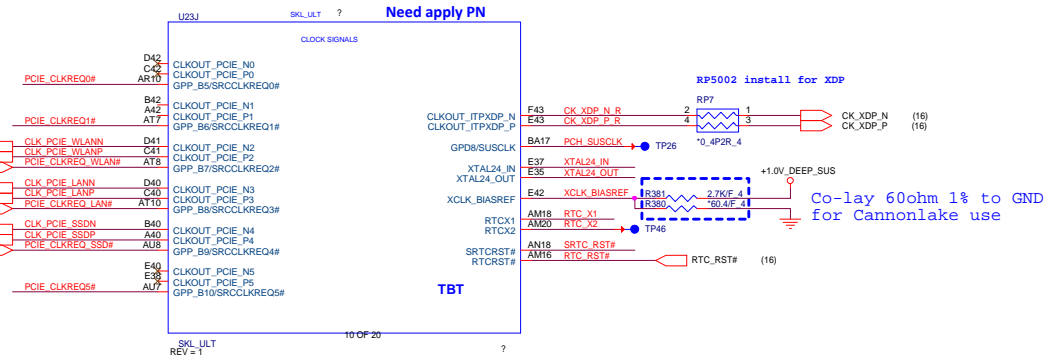
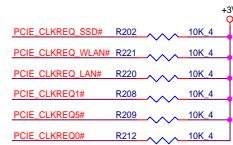
+3V_RTC_2 (4,15)
 +3V_RTC (4,15)
 +3V (2,4,10,11,12,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,32,34,38,40)
 +1.0V_DEEP_SUS (9,15,16,38,40,44)

WLAN

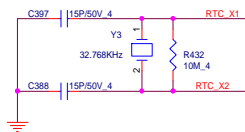
LAN

SSD

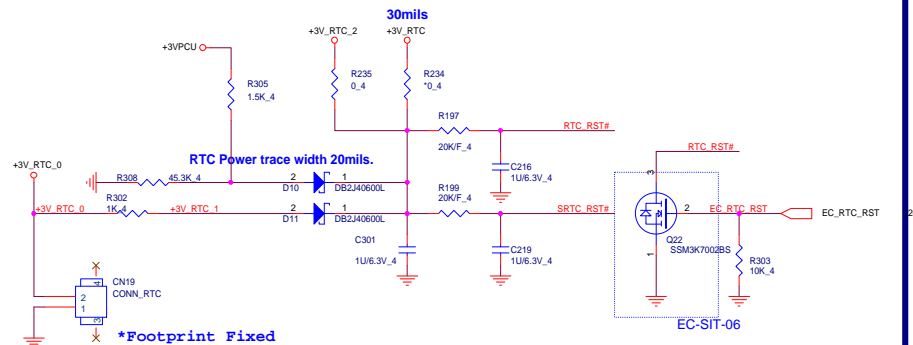
CLK_REQ/Strap Pin(CLG)



RTC Clock 32.768KHz

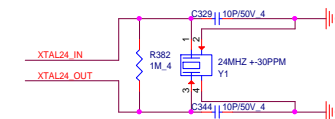


RTC Circuitry(RTC)



External Crystal and Green Clock

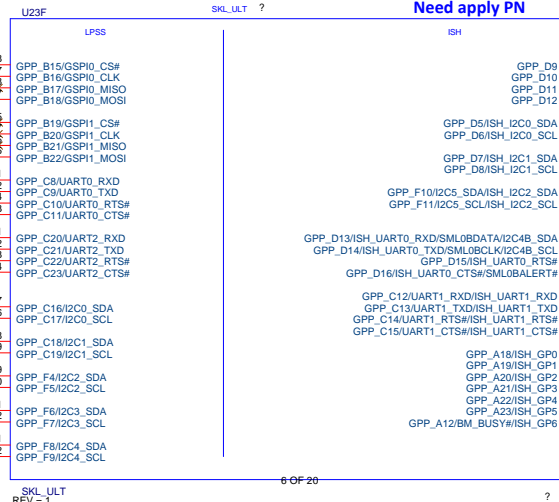
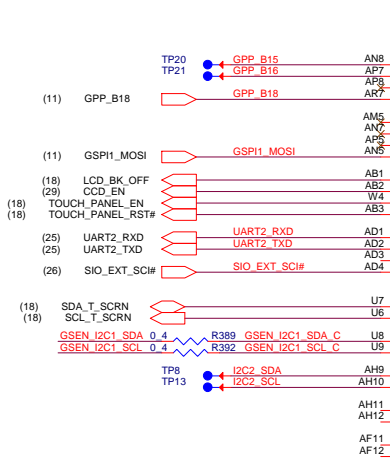
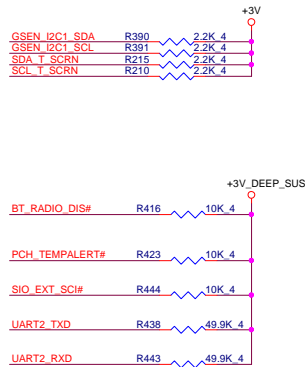
The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



30 ppm required

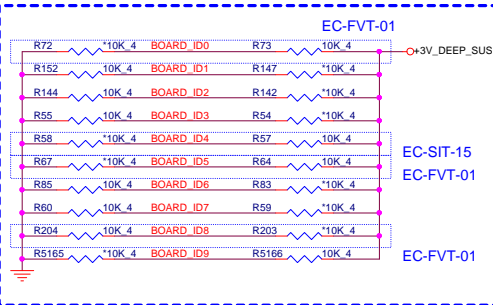
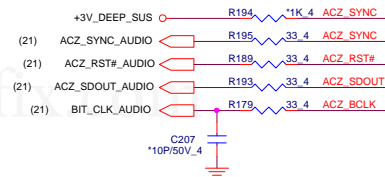
Skylake (GPIO)

+3V (2,4,10,11,12,13,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,32,34,38,40)
+3V_DEEP_SUS (2,4,10,11,12,15,16)



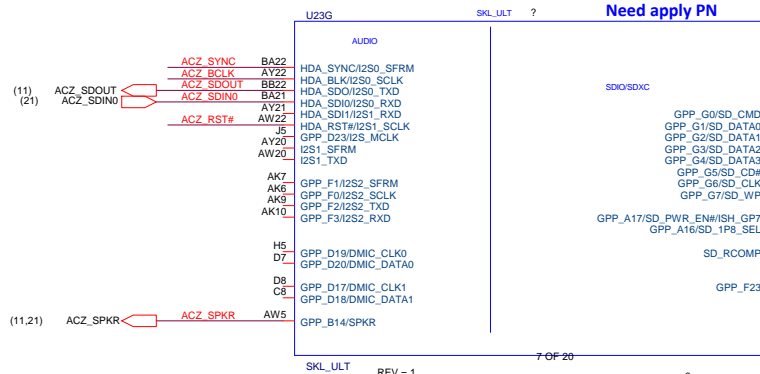
* Please be noted ISH_GP[0:7] (Multiplexed with GPP_A12, GPP_A17, GPP_A[18:23]) are in PCH Primary Well Group A, when eSPI (Multiple xed with GPP_A[0:15]) is enable, VCCPGPPA should be supplied by 1.8V. That means the signaling level of all the Primary Well Group A signals including ISH_GP[0:7] will be 1.8V.

HDA Bus(CLG)



Stage	SKU	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
Bring up	Touch SKU	0	0	0	0	0	1
	Non-Touch	0	0	0	0	0	0
SDV/FVT	Touch SKU	1	0	0	0	0	1
	Non-Touch	1	0	0	0	0	0
SIT	Touch SKU	1	1	0	0	0	1
	Non-Touch	1	1	0	0	0	0
SOVP	Touch SKU	1	1	0	0	0	1
	Non-Touch	1	1	0	0	0	0

Model	LI8K/L	PS9
BOARD_ID9	1	0



Vinafix.com

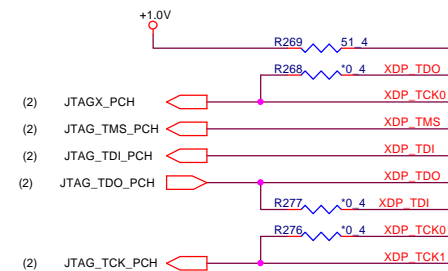
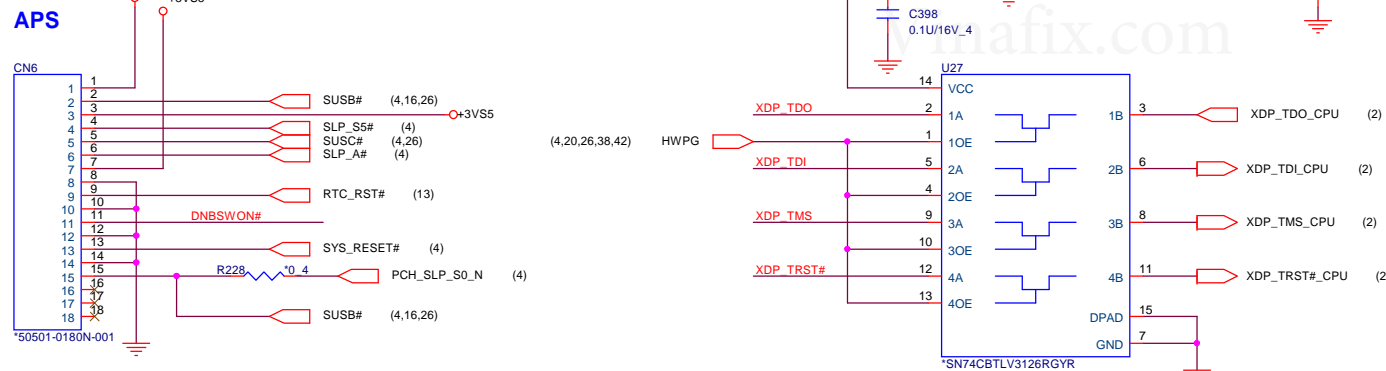
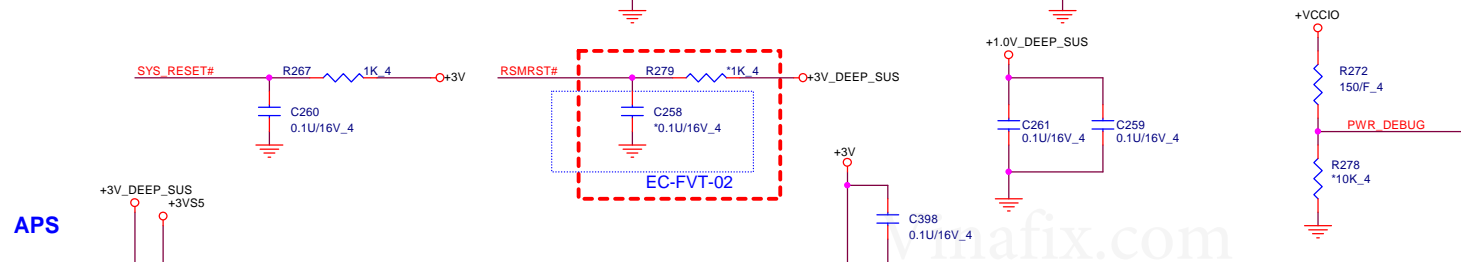
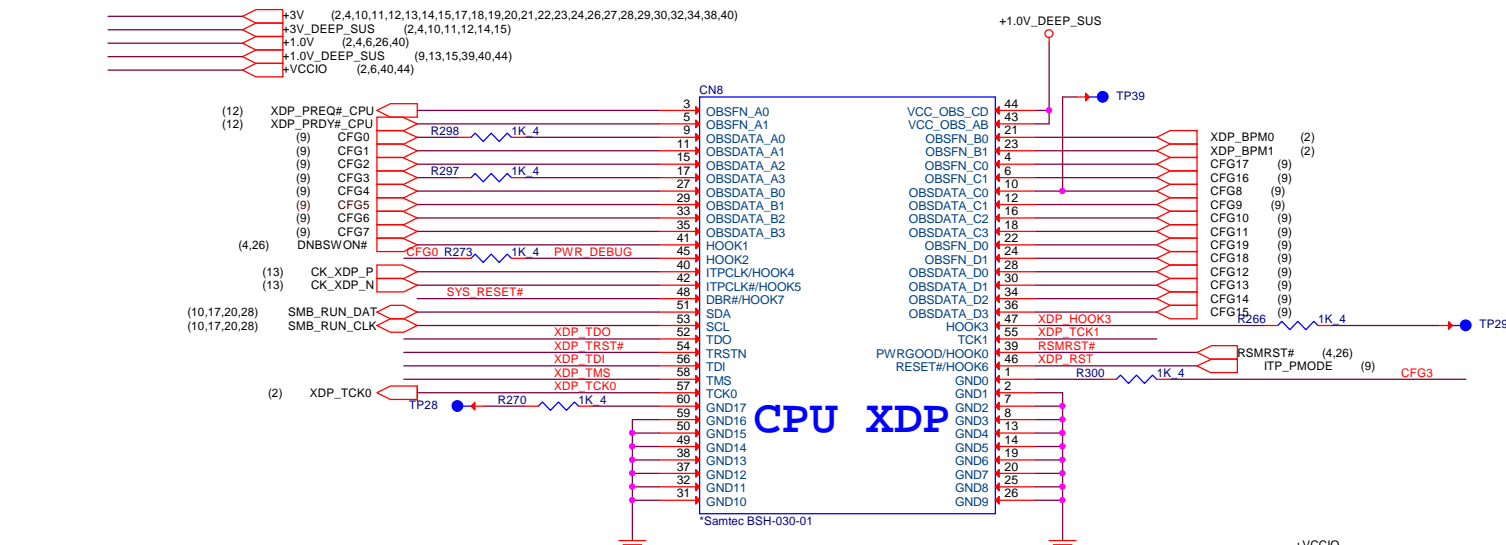
Proposed location must be under the keyboard (TOP side)

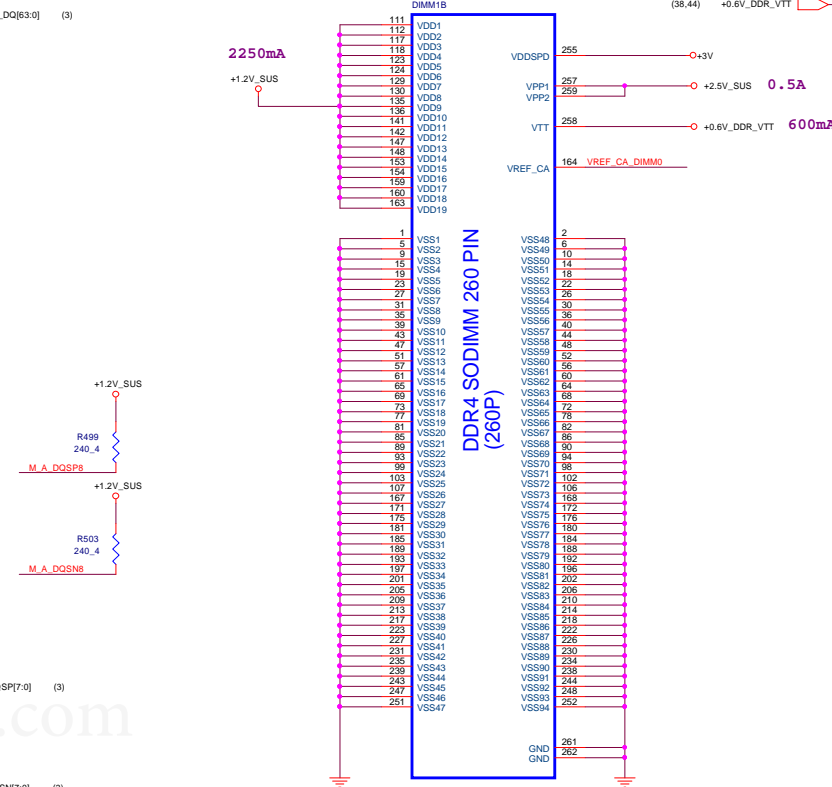
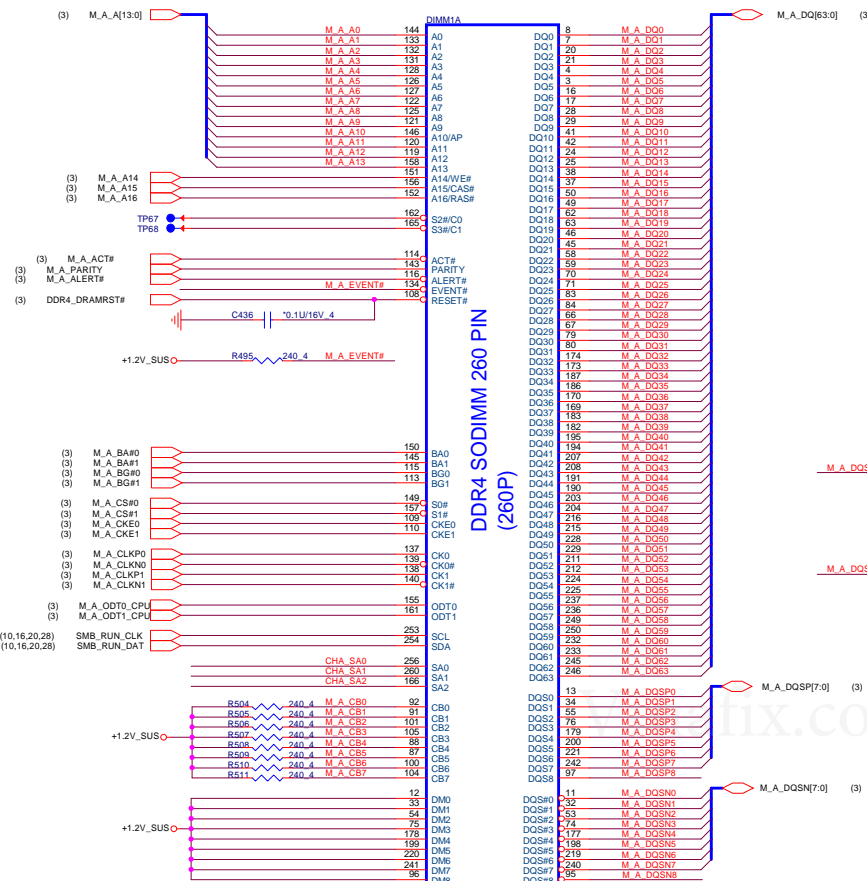


PROJECT : LI8K
Quanta Computer Inc.

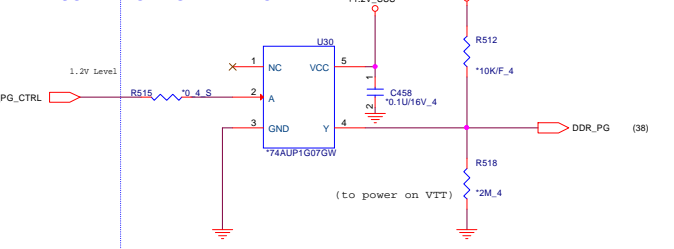
Size Document Number 14 -- SKYPAKE 19/20 (GPIO) Rev 3A
Date: Thursday, September 08, 2016 Sheet 14 of 45





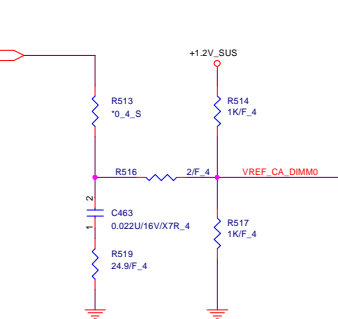


DDR4 SODIMM ODT GENERATION

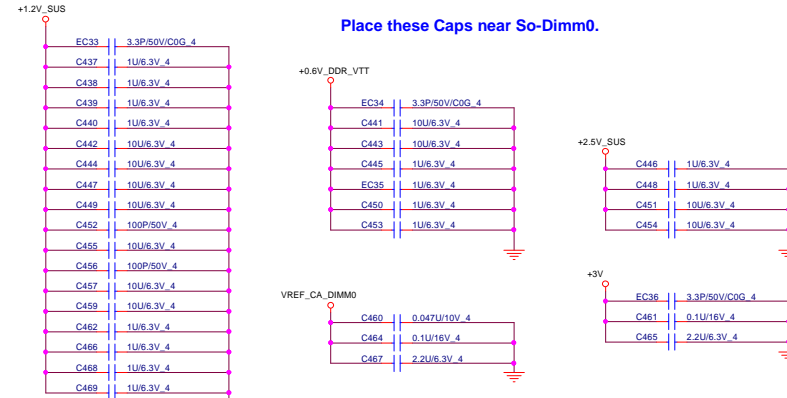


EC-SIT-11

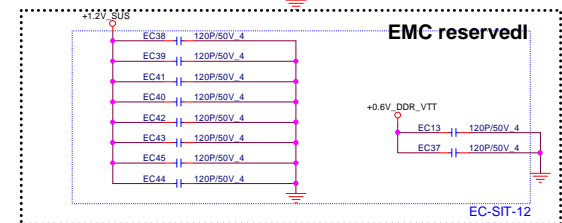
VREF CA DIMMO Solution



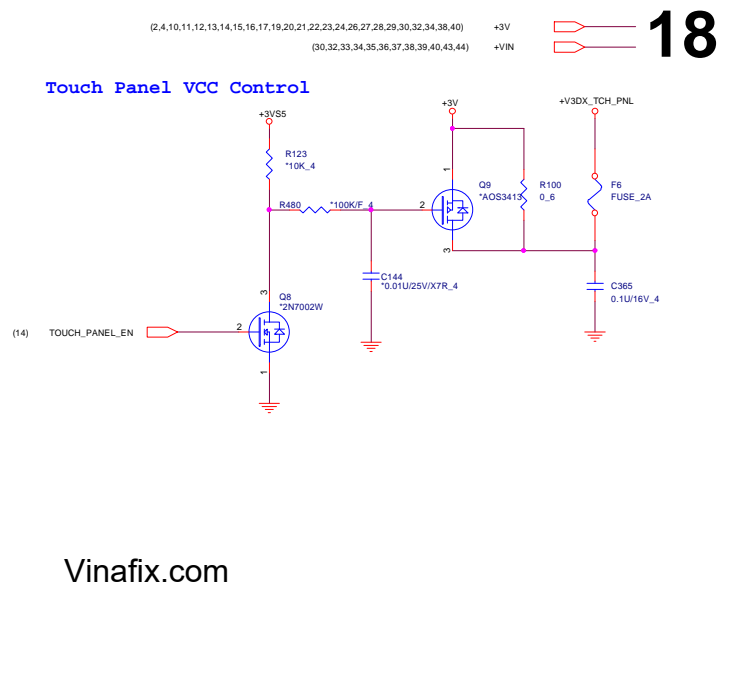
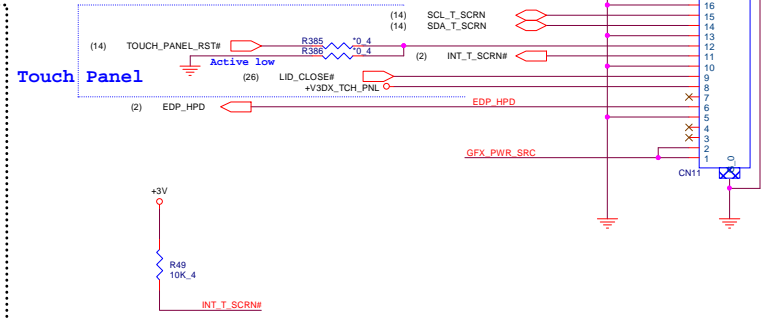
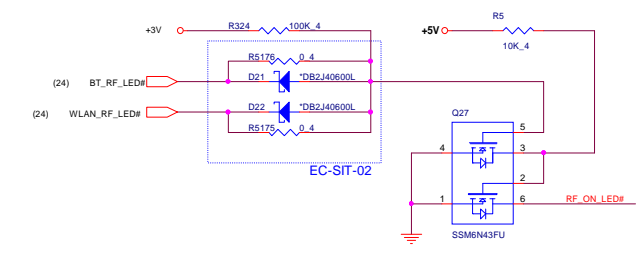
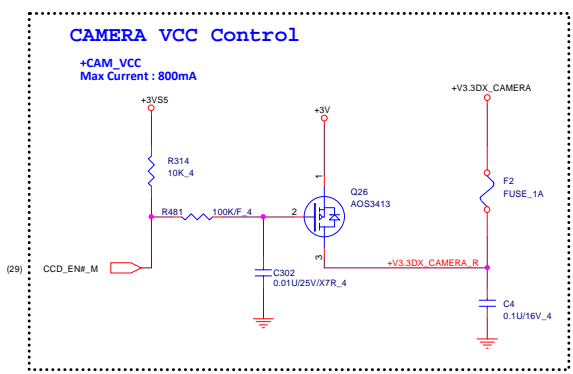
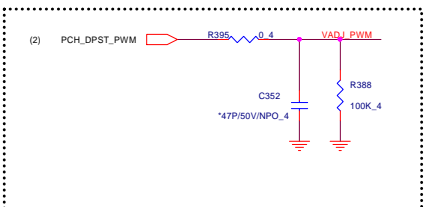
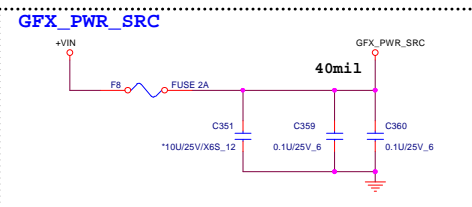
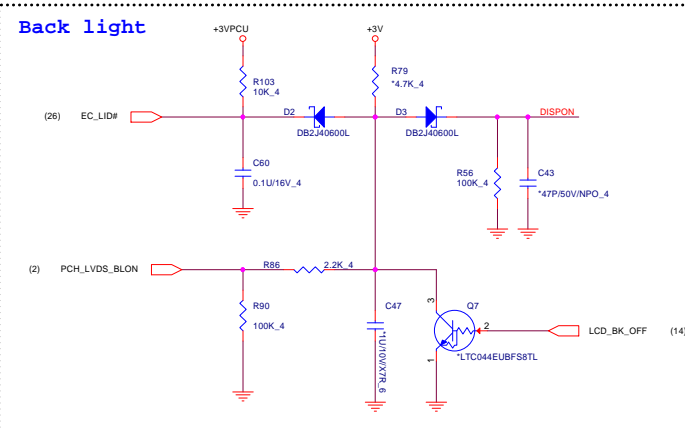
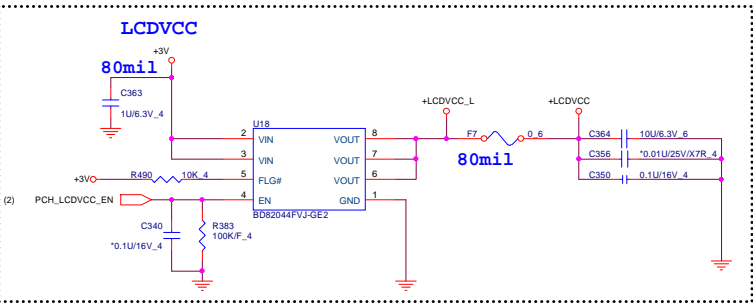
Place these Caps near So-Dimm0.



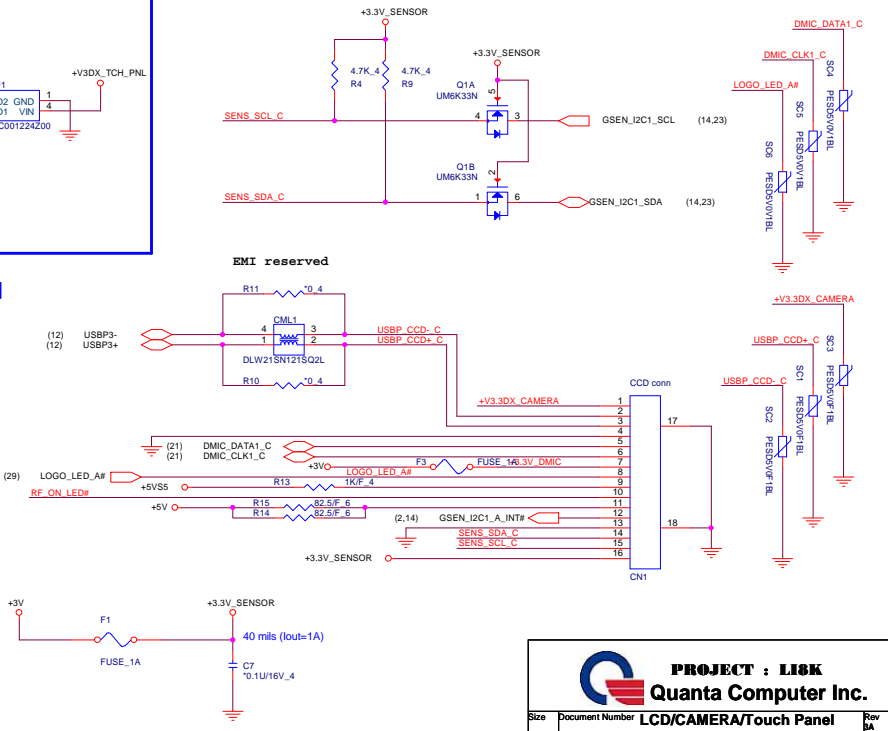
EMC reserved!

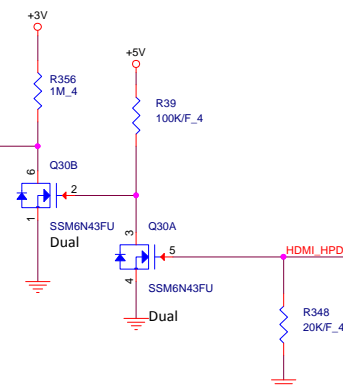


EC-SIT-12

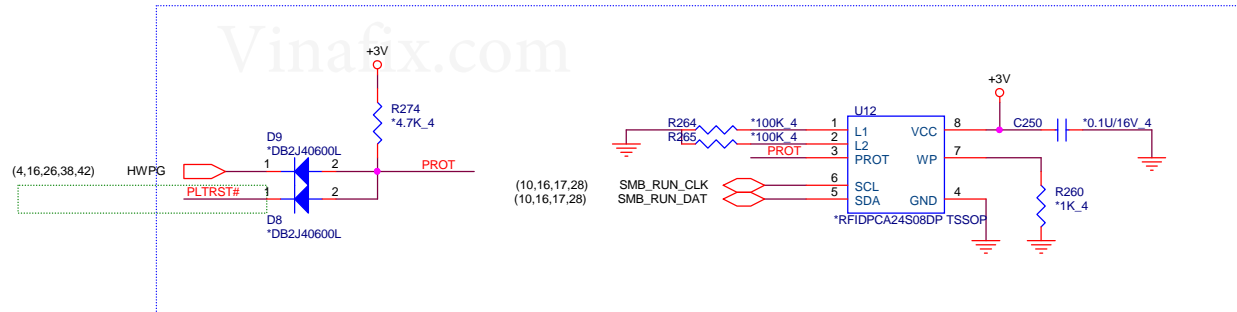
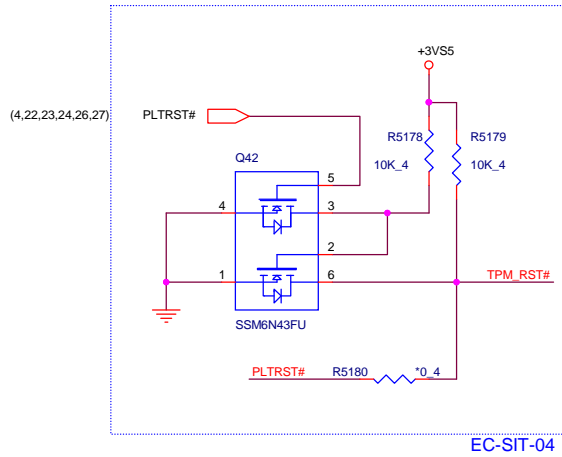
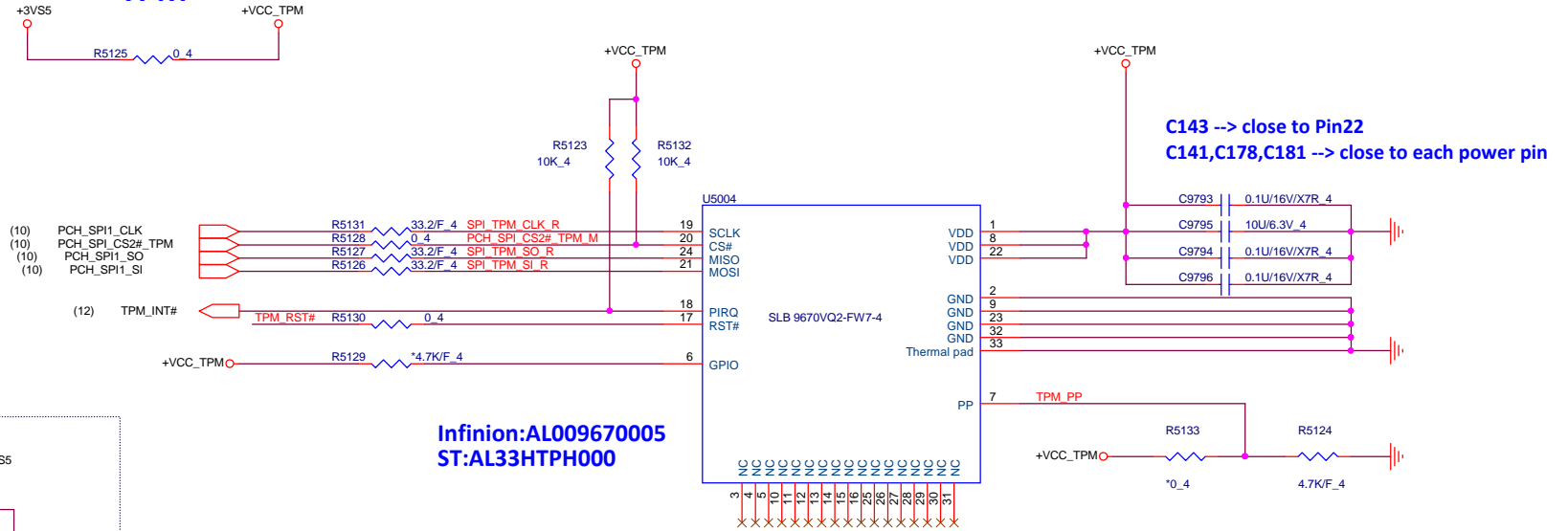


CCD+MIC+LOGO+WLAN LED CONN





TPM



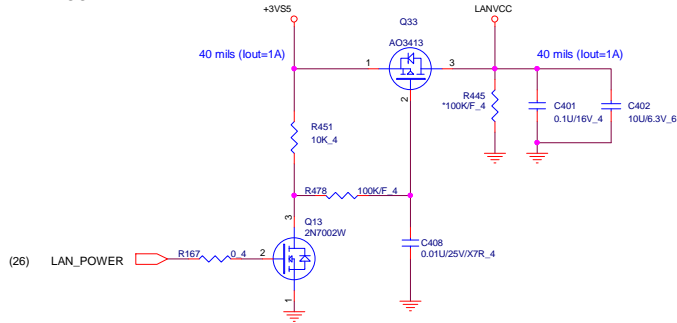
PROJECT : L18K
Quanta Computer Inc.

Size	Document Number	Rev
	TPM/RFID	3A
Date:	Thursday, September 08, 2016	Sheet 20 of 45

21

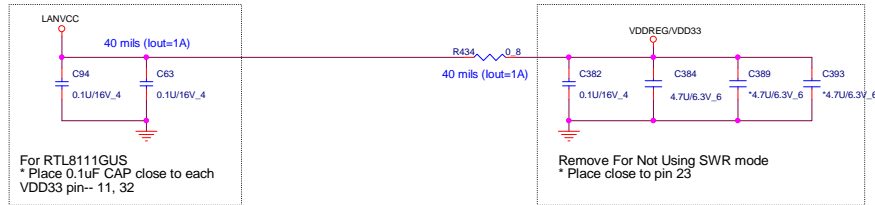


LANVCC



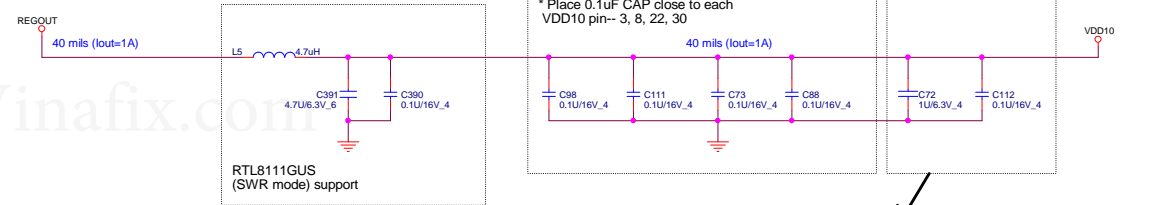
LANVCC
Trace width>60mil,
Trace length<200mil

Vinafix.com



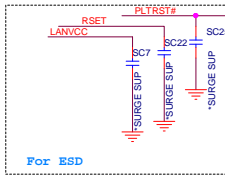
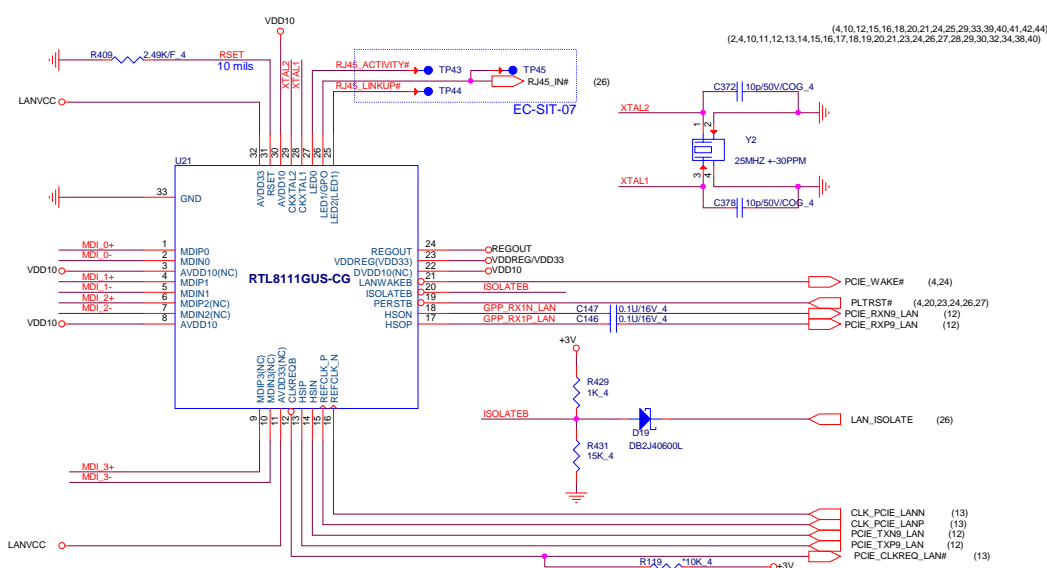
For RTL8111GUS
* Place 0.1uF CAP close to each
VDD33 pin-- 11, 32

Remove For Not Using SWR mode
* Place close to pin 23



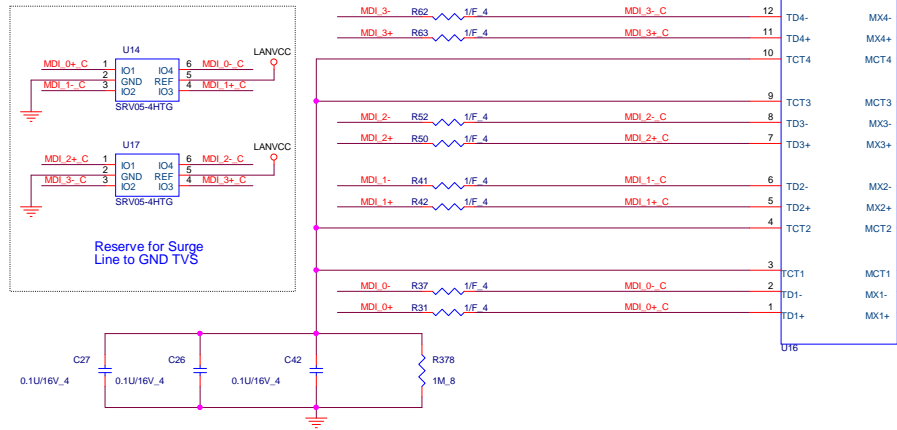
For RTL8111GUS
* Place 0.1uF CAP close to each
VDD10 pin-- 3, 8, 22, 30

For RTL8111GUS
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)



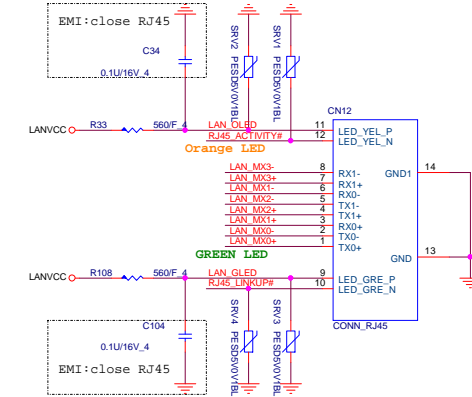
For ESD

Transformer



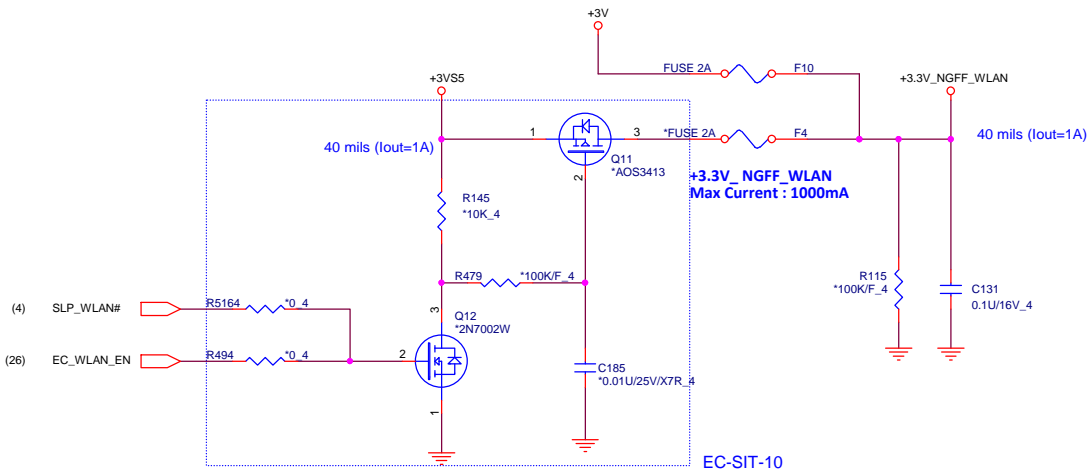
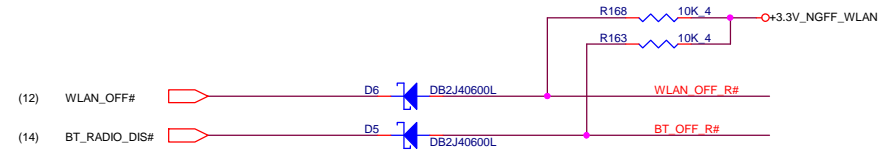
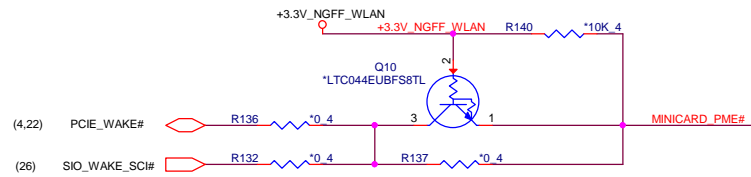
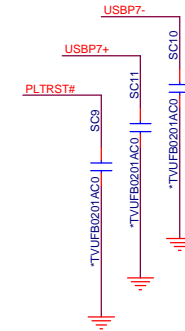
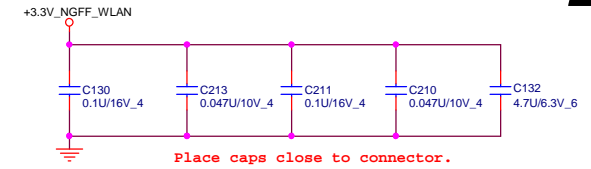
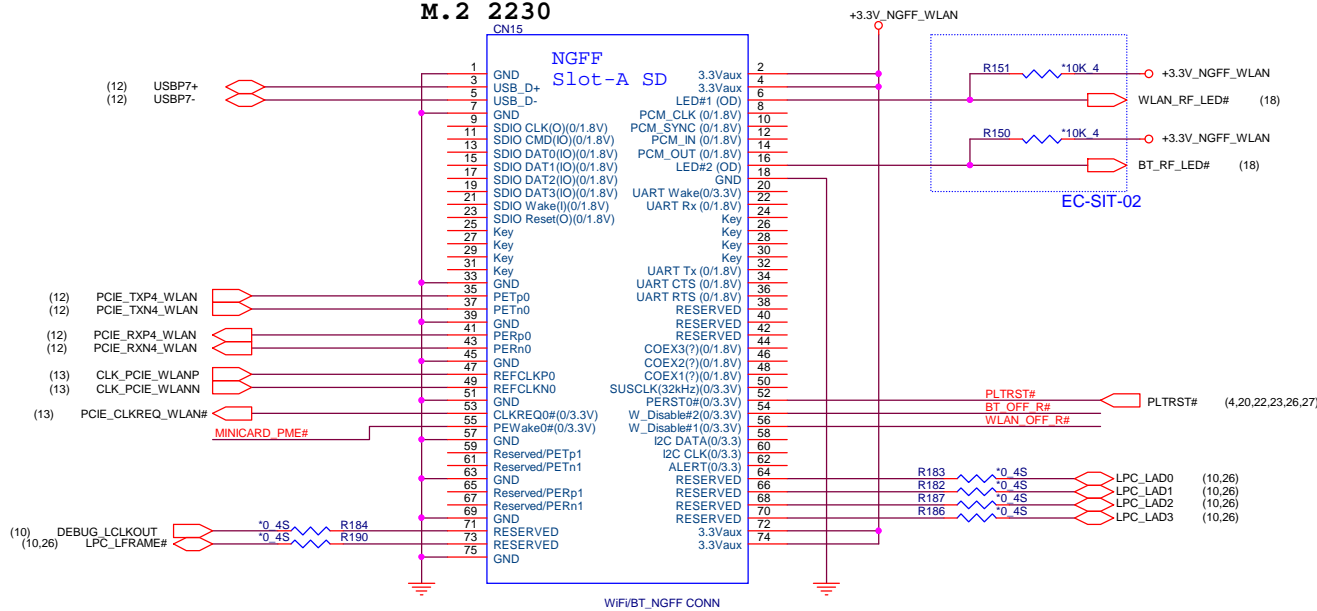
Layout: All termination
signal should have 50 mil
trace / 50mil spacing

RJ45 Connector

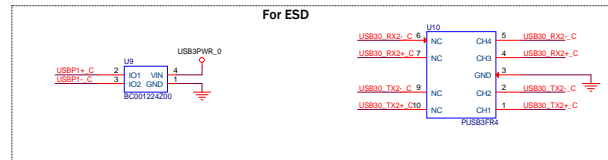
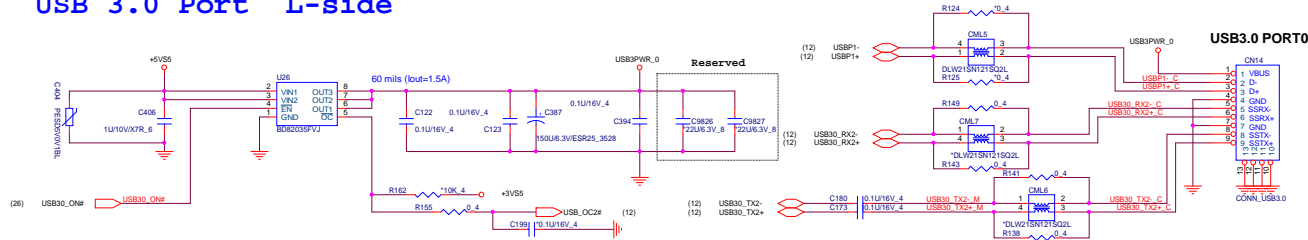




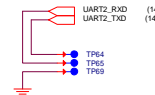
NGFF WiFi/BT connector M.2 2230



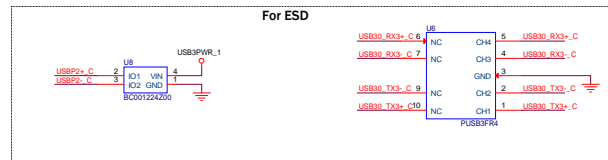
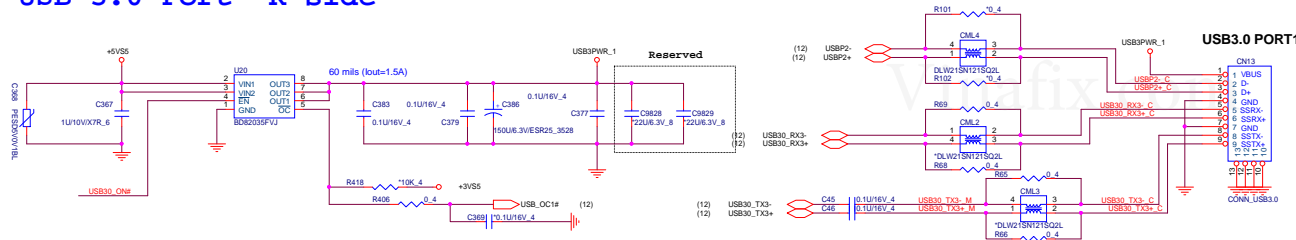
USB 3.0 Port L-side



UART for DEBUG

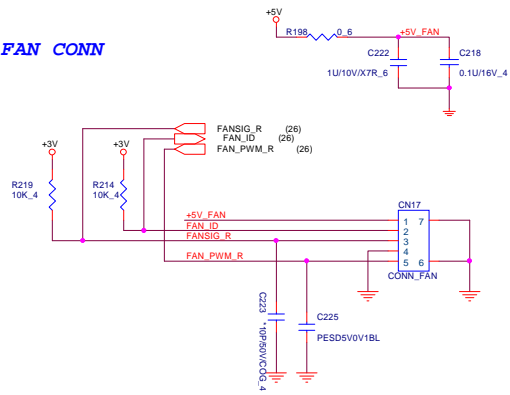


USB 3.0 Port R-side

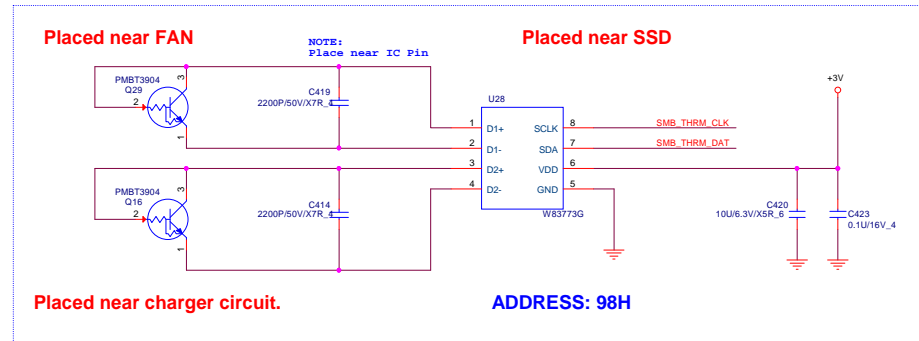




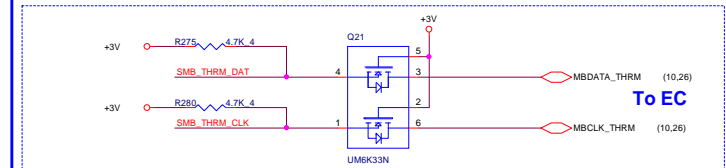
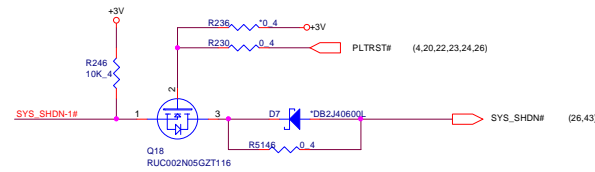
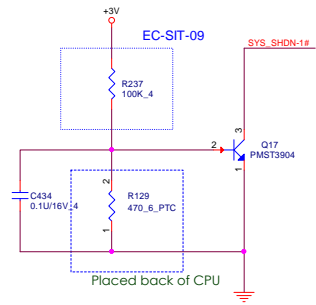
FAN CONN



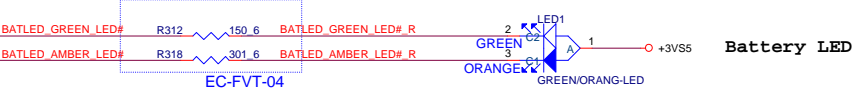
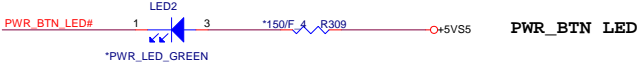
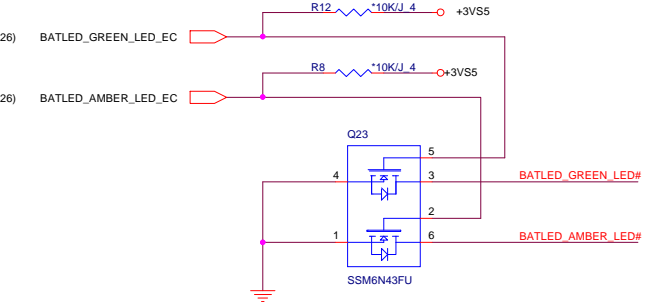
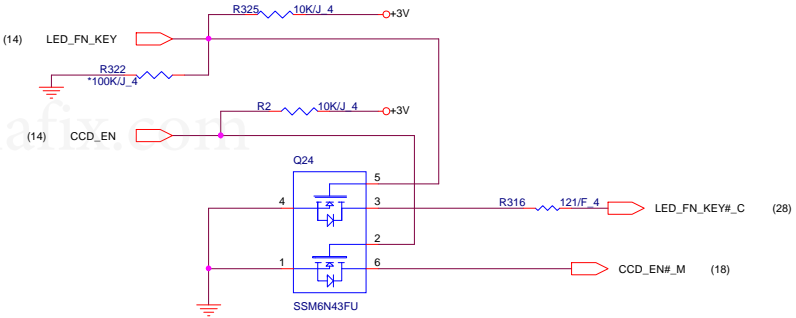
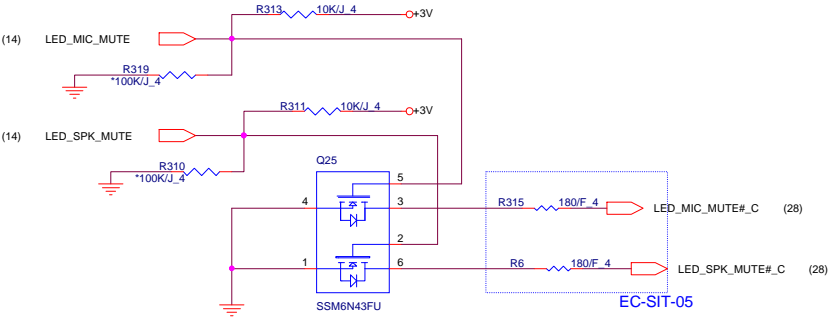
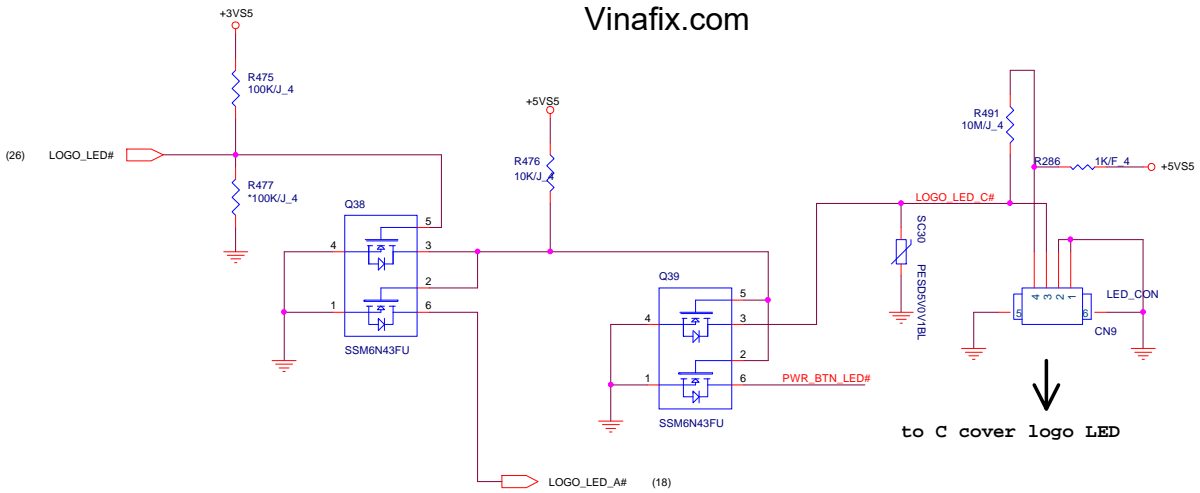
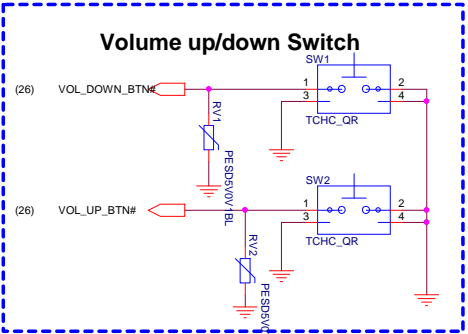
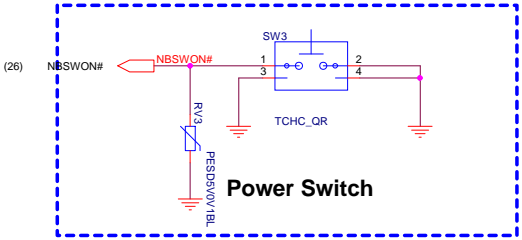
Thermal Sensor

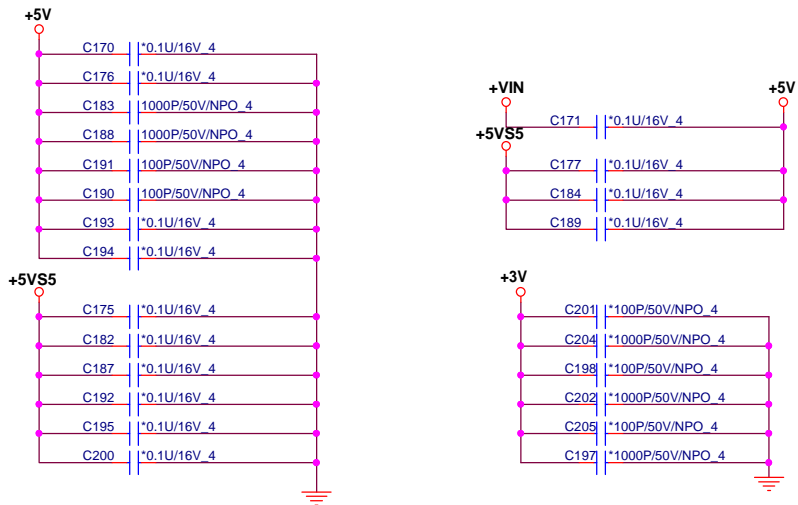


CPU PTC circuit




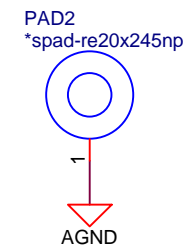
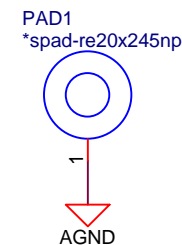
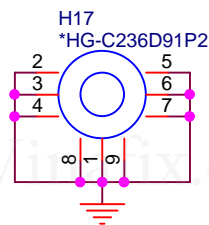
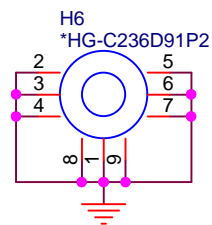
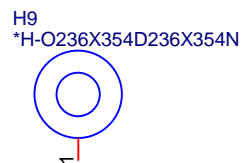
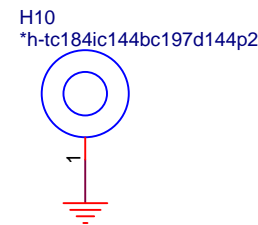
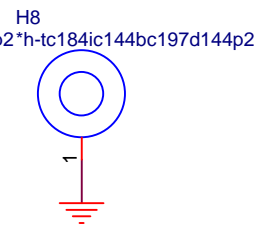
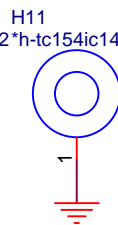
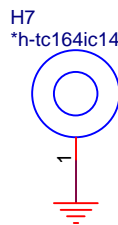
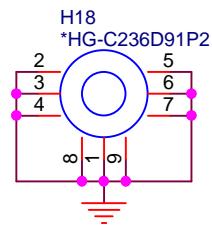
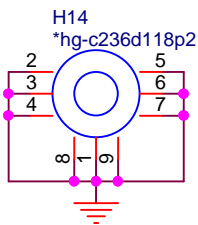
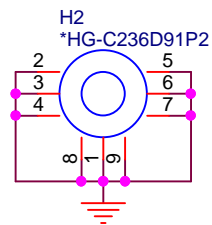
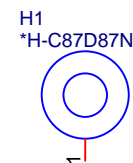
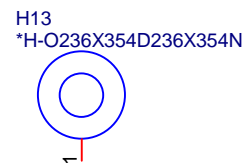
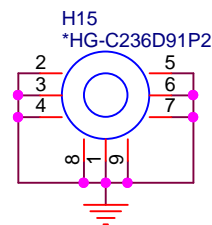
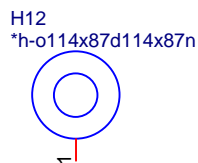
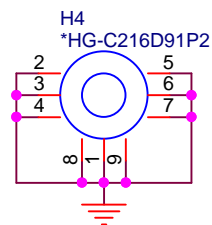
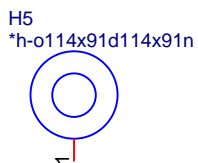
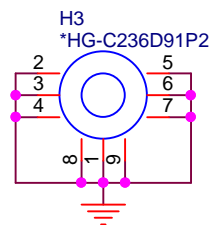
LED Driver



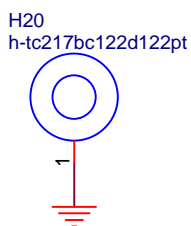
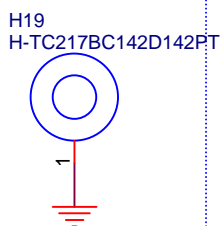


Vinafix.com

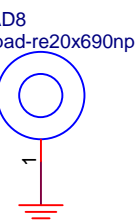
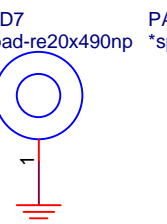
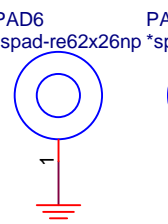
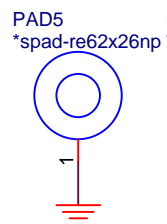
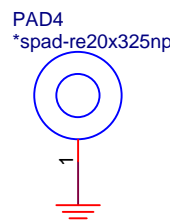
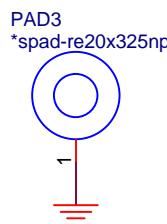
 PROJECT : LI8K Quanta Computer Inc.		Rev 3A
Date: Thursday, September 08, 2016		Sheet 30 of 45



Stuff NUT Location:

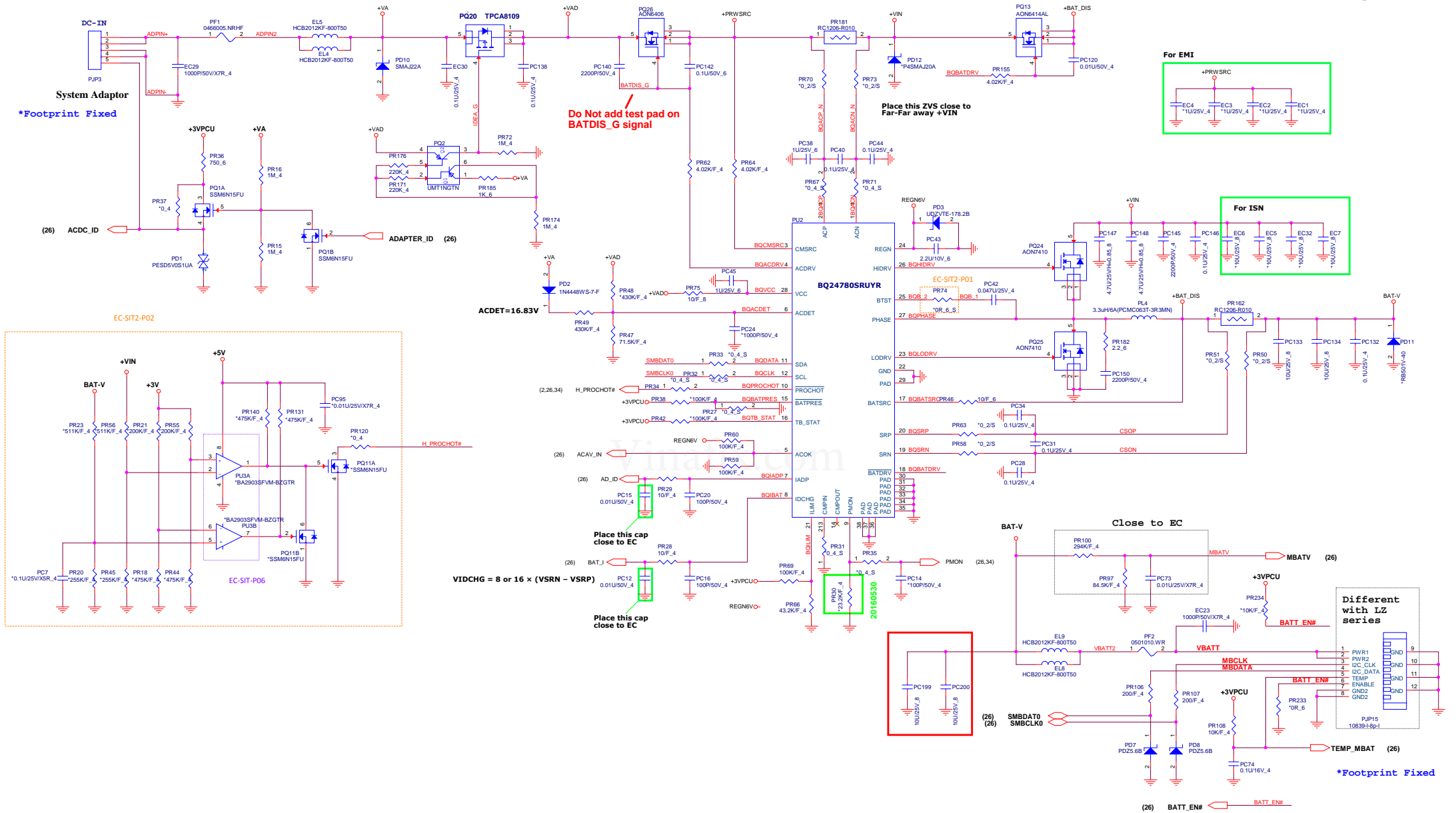


EC-DV-08
EC-SIT2-10

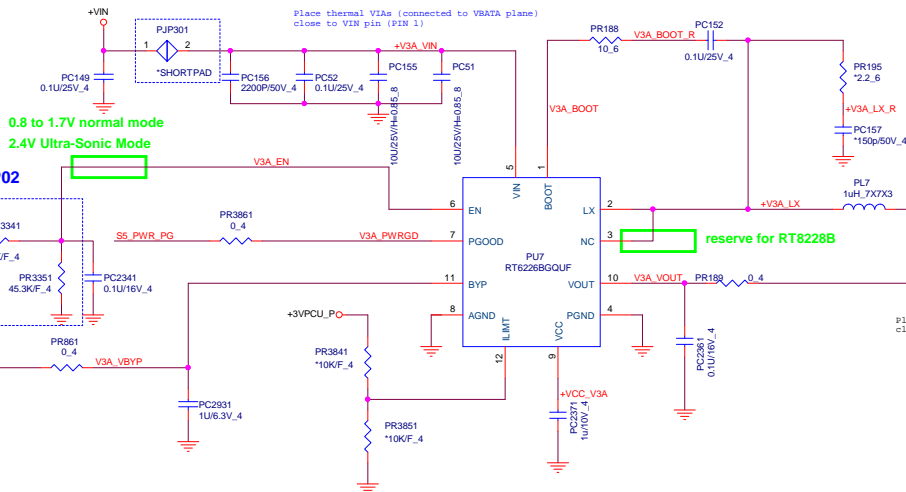


PROJECT : LI8K
Quanta Computer Inc.

Size A	Document Number	Screw Hole	Rev 3A
Date:	Thursday, September 08, 2016	Sheet 31 of 45	

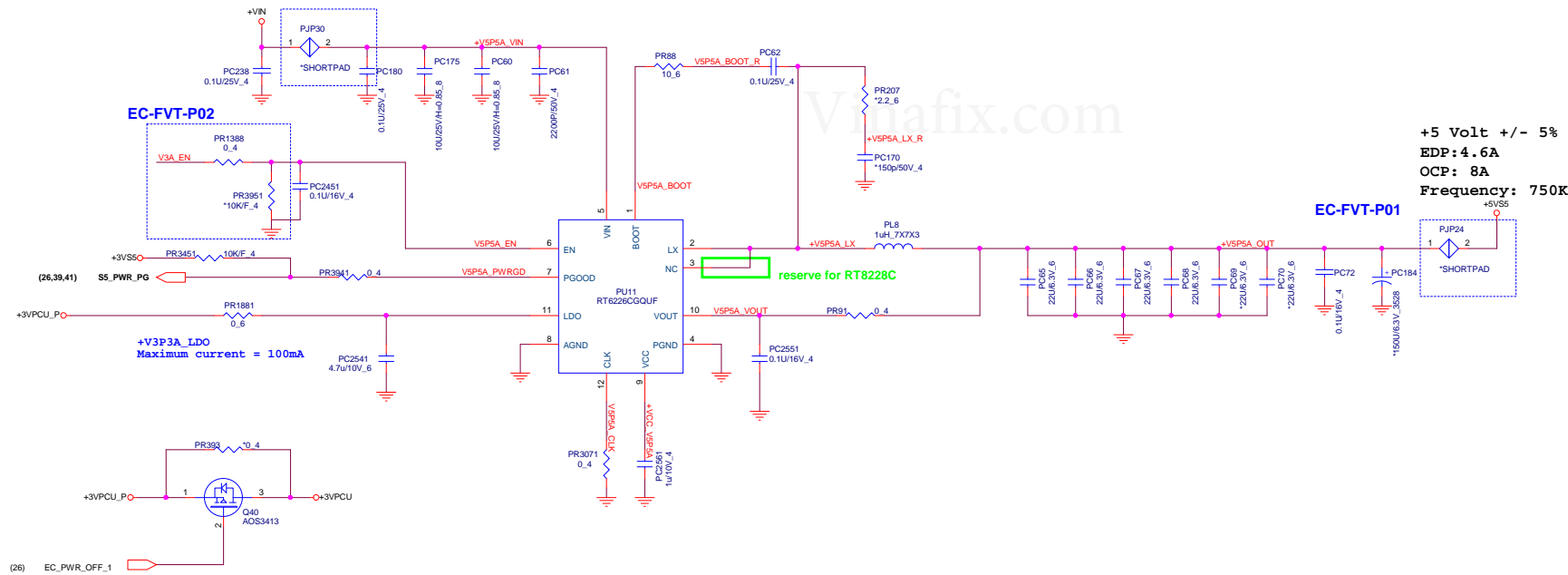


EC-FVT-P01

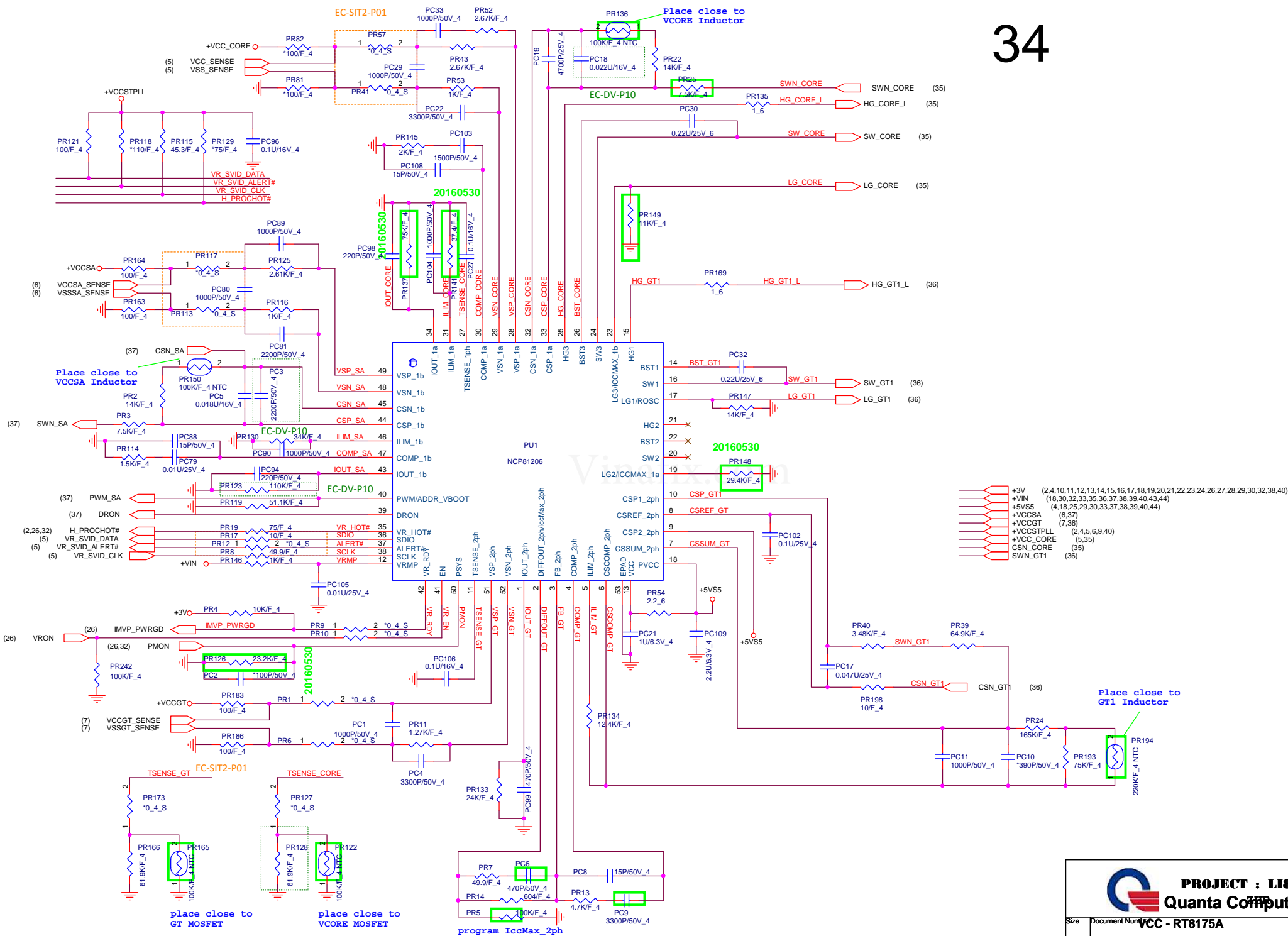


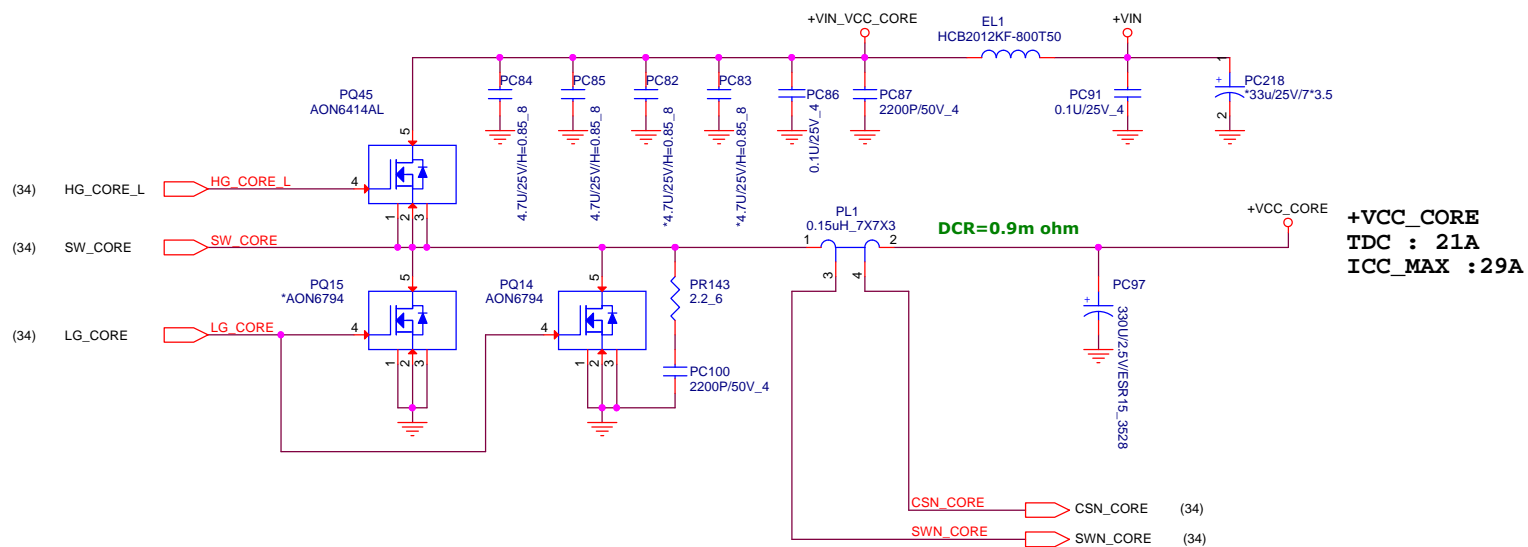
Vinafix.com

EC-FVT-P01



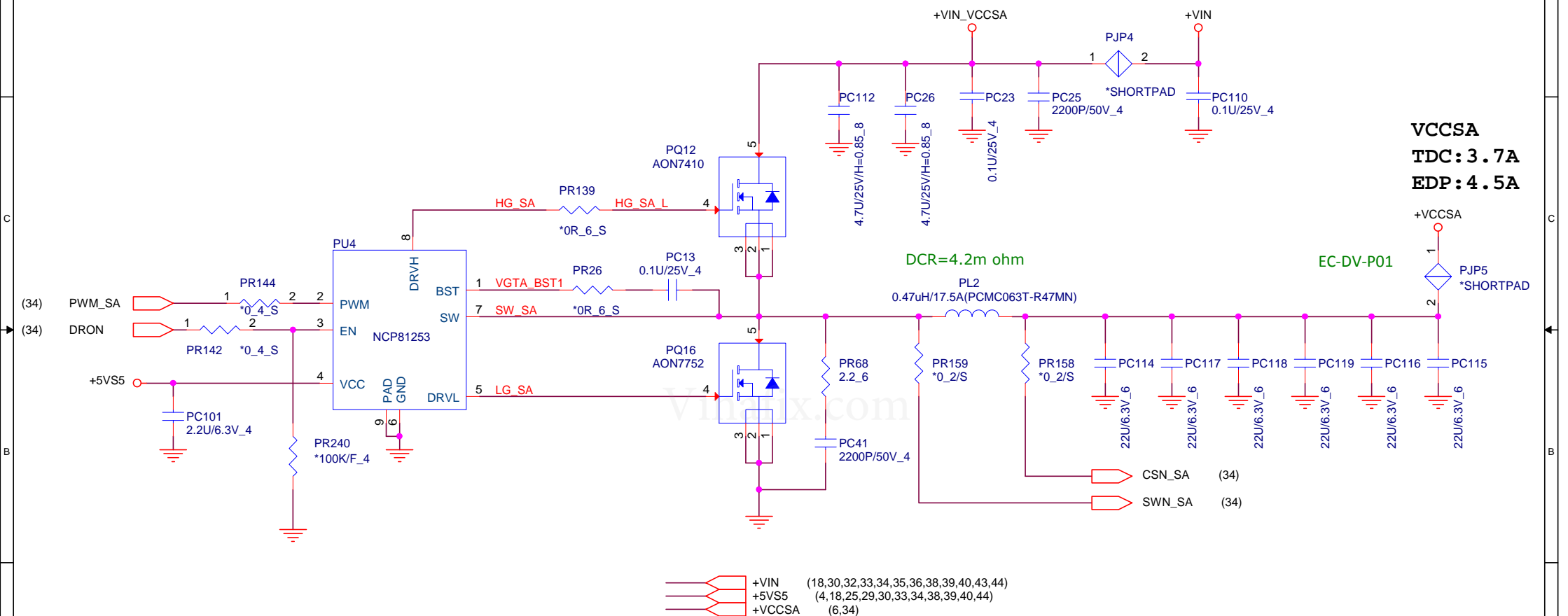
PROJECT : L18K
Quanta Computer Inc.






Vinafix.com

VCCSA
TDC: 3.7A
EDP: 4.5A



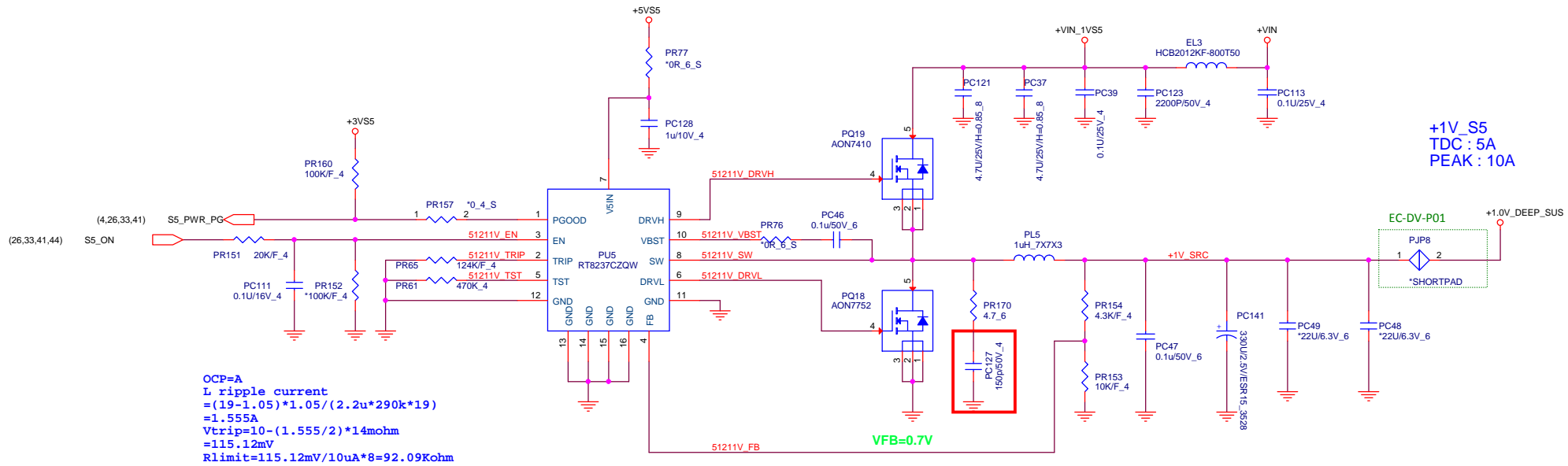
Vinafix.com

 PROJECT : LI8K Quanta Computer Inc.		<Rev Code>
CustomDoc	Document Number	
Date:	Thursday, September 08, 2016	Sheet 37 of 45



PROJECT : LI8K
Quanta Computer Inc.

Size	Document Number	ZHR	RevA
	+VBATA		
Date:	Thursday, September 08, 2016	Sheet	0 of 0

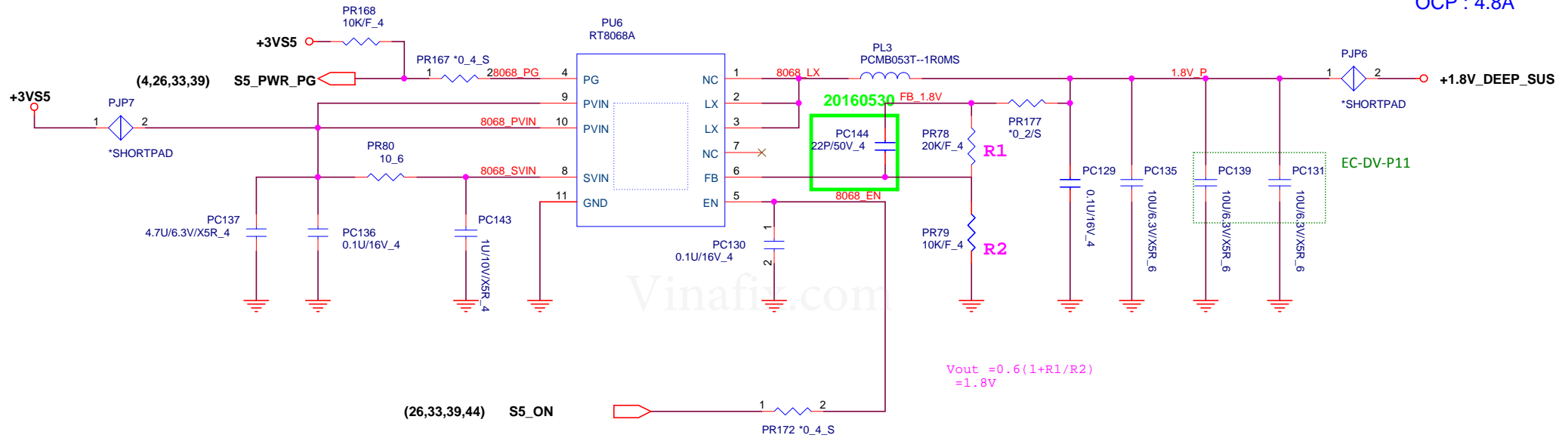



Vinafix.com

V1P8A (RT8068A)

Vinafix.com

1.8V_S5
Fsw : 900KHz
PEAK : 0.27A
OCP : 4.8A



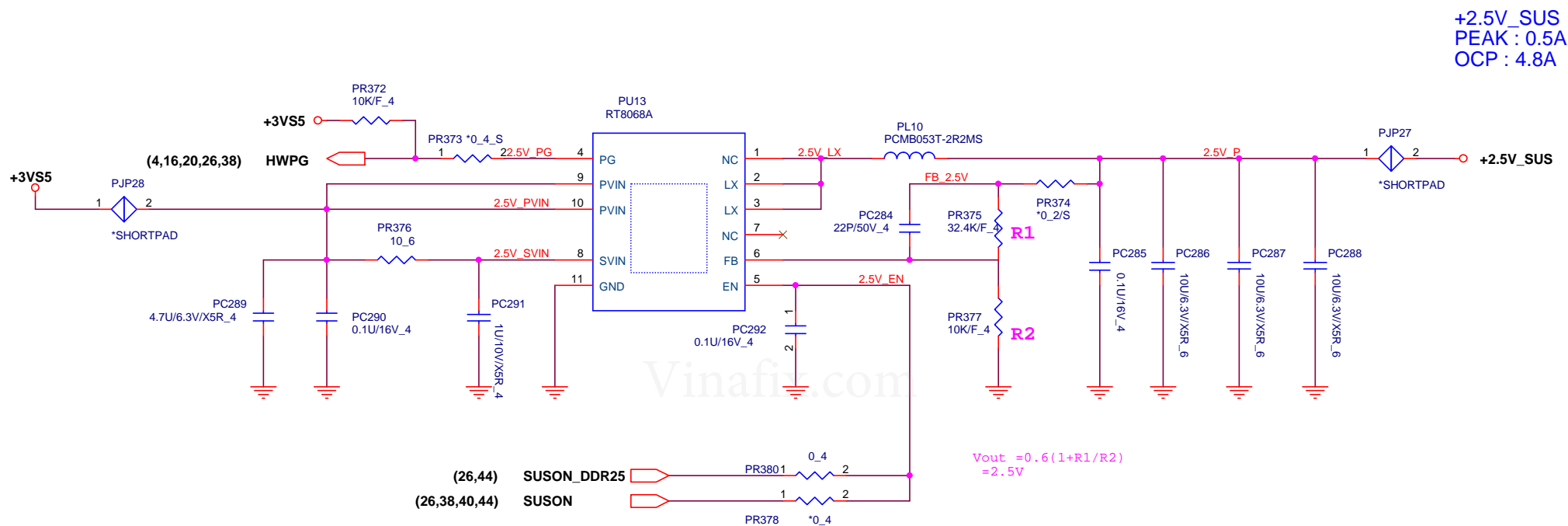


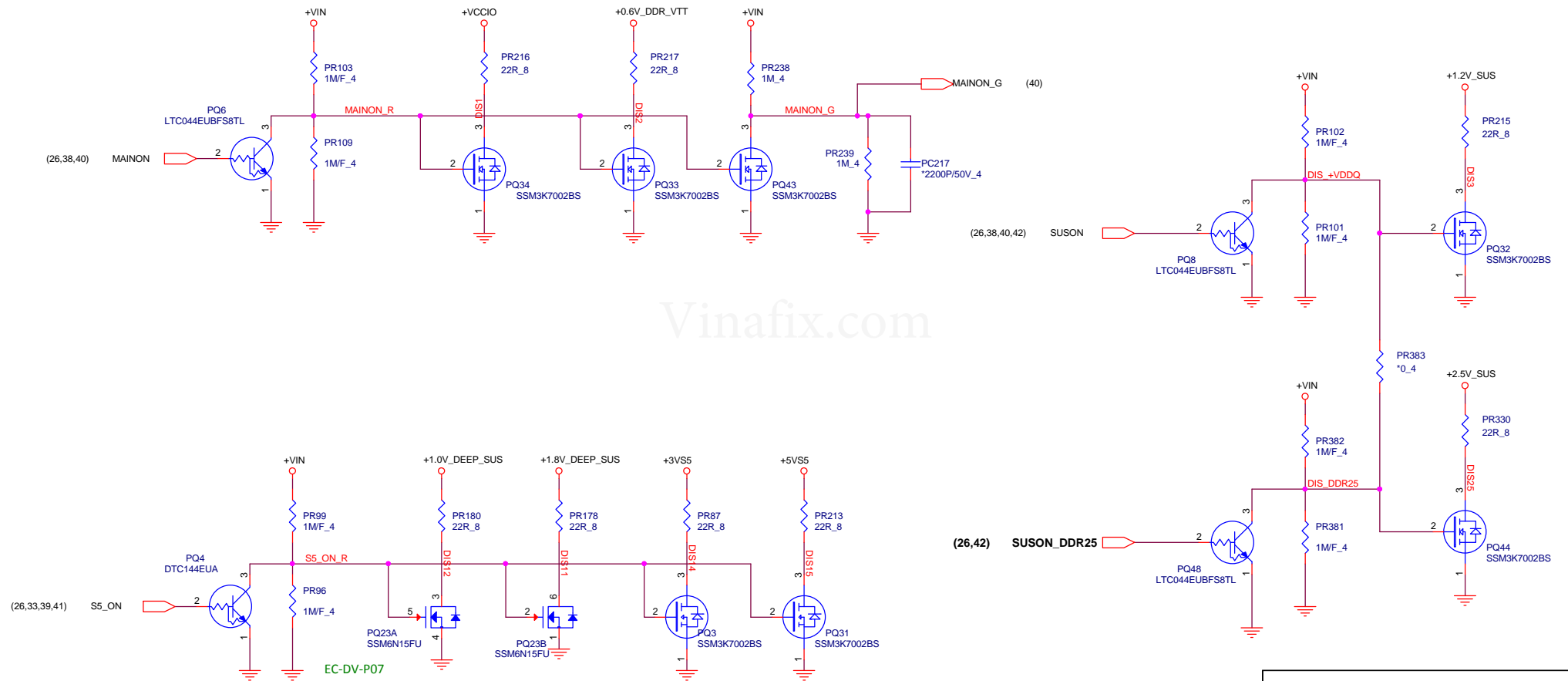
PROJECT : LI8K

Quanta Computer Inc.

CustomDoc		<RevCoc>
Size	Document Number	Rev
Date: Thursday, September 08, 2016		Sheet 41 of 45

2.5V (RT8068A)



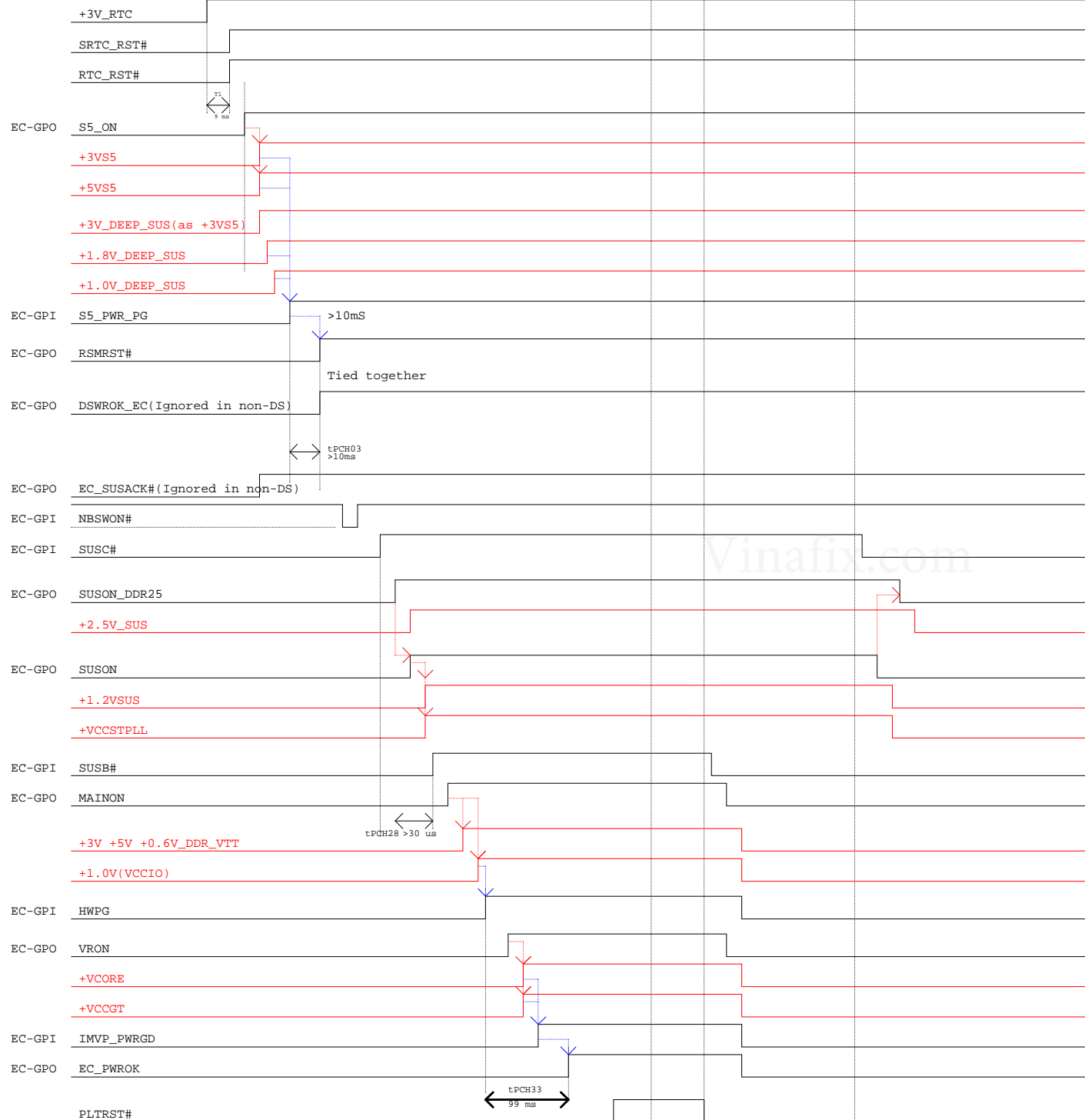


G3 to S0

S0

S0 to S3

S4/S5



Intel POWER UP SEQUENCE

Vinafix.com

LI8K EE Schematic EC Tracking Record FVT to SIT version

EC #	Page	Description	Part Affected
EC-SIT-01	21	Reserved 0 ohm resistor for Enhanced PC Beep	Reserved: R5174
EC-SIT-02	18	Change the RF LED control path to 0 ohm component due to over dsign.	Add: R5175,R5176 Remove: D21,D22,R150,R151
EC-SIT-03	26	Add force disable circuit for EC reset 3VPCU knee voltage issue	Add: Q37,R5177
EC-SIT-04	20	Add reset circuit for ST TPM can boot issue.	Add: Q42,R5178,R5179
EC-SIT-05	29	Change KB LED current limit resistor 150 to 180 for Chicony KB	R6,R315
EC-SIT-05	13	Stuff RTC_RST circuit.	Q22
EC-SIT-06	4	Add driving low path for RTC corruption issue while surprise power loss.	D25,R5183 Reserved: Q43
EC-SIT-07	22,26	Add the RJ45_IN# path for "Wireless Auto Disconnection"	R5181
EC-SIT-08	26	Add the BATT_EN# path for battery enabling by EC	R5182
EC-SIT-09	27	Fine tune the thernall protection.	R237
EC-SIT-10	24	Remove reserved parts	Remove: Q11,Q12,R5164,R145,R479,C185
EC-SIT-11	17	Remove reserved parts	Remove: U30,C458,R512,R518
EC-SIT-12	17	Add EMC suggestion	Add: EC38,EC39,EC40,EC41,EC42,EC43,EC44,EC45,EC13,EC37
EC-SIT-13	23	Cancel NVME SSD support	Remove: C264,C265,C270,C271.C267,C268 Change: C256,C257,C262,C266
EC-SIT-14	21	Change resistor to fine tune PCBEEP volume.	R247
EC-SIT-15	14	Change BID for SIT identification	R57,R58
EC-SIT-16	21	Add 680p cap for KCC test.	R462,R467



PROJECT : LI8K
Quanta Computer Inc.